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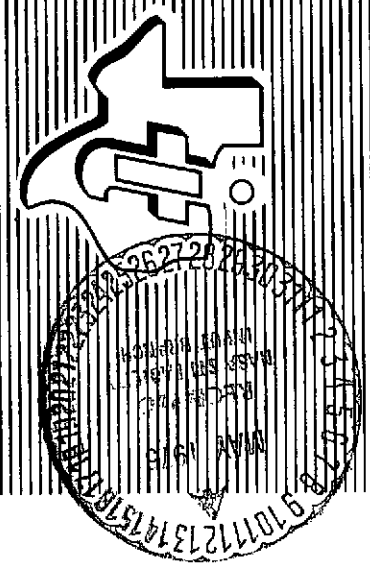

FINAL REPORT
S-BAND ANTENNA PHASED ARRAY COMMUNICATIONS SYSTEM

NASA CR-
141756

Prepared for:

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Space Administration
Lyndon B. Johnson Space Center
Houston, Texas

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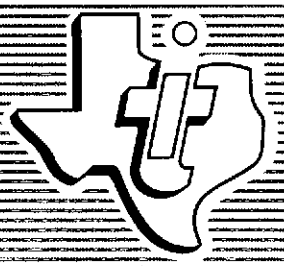

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March 1975

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This final report describes the results of a design-development effort performed by Texas Instruments for NASA/Lyndon B. Johnson Space Center under Contract NAS9-14196. Texas Instruments appreciates the opportunity to have performed this contract, and hopes NASA finds the information in this report complete and useful.

Texas Instruments' program manager for this effort was Dr. Dennis R. Delzer. Other major contributors were:

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Texas Instruments will welcome the opportunity to expand the technical foundation laid in this effort. We are confident that continued development of the spacecraft antenna array described herein will lead to a very useful subsystem applicable to a number of spacecraft uses.

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March 1975

FINAL REPORT
S-BAND ANTENNA PHASED ARRAY COMMUNICATIONS SYSTEM

SECTION I

INTRODUCTION

This report contains the results of the first phase of the S-Band Antenna Phased Array Communications System (SPACS I) program sponsored by the Electromagnetic Systems Branch of NASA Lyndon B. Johnson Space Center under contract NAS9-14196. The system requirements, a detailed antenna array subsystem design, and details of the hardware implementation will be discussed in this report.

Many instances of spacecraft-to-spacecraft communications (e.g., spacecraft/relay satellite and shuttle/payload) may require a medium amount of antenna gain for successful implementation. Of the two approaches to achieving antenna gain (i.e., mechanically steered reflector or electronically steered phased array), the phased array approach offers the greatest simplicity and lowest cost (size, weight, power, and dollars) for this medium gain. This report describes a competitive system design as well as hardware evaluation which will lead to timely availability of this technology for implementing such a system.

The objectives of the SPACS I contract are:

- To design a proposed (flight model) medium gain active phased array S-band communications antenna subsystem,
- To develop and test one breadboard seven-element planar array (antenna) of radiating elements mounted in the appropriate cavity matrix,

- To develop and test one breadboard transmit/receive microelectronics module.

The development requirements under this contract consisted of making required modification and/or additions to transmitter/receiver and antenna designs previously developed under NASA contract NAS8-25847 with Marshall Space Flight Center. The technology developed under this previous contract was utilized to the maximum extent that it fit JSC design requirements. Areas where additional development was required were investigated and breadboarded to the extent required by the specifications.

The work tasks were divided into three major areas. The first major task is that of Hardware Definition. This task consisted of evaluation of basic system requirements, trade-off studies, thermal analysis and hardware evaluation. The second major task is that of Critical Item Development. This task consisted of breadboarding and evaluation of those items in the design considered to be the most critical to the program. The third and last major task consisted of the actual breadboarding of one complete transmit/receive module (containing phasors) along with one array of seven antennas.

SECTION II

ANTENNA ARRAY SUBSYSTEM REQUIREMENTS

The antenna array subsystem requirements are based upon the set of system parameters outlined in Table 2-1. These requirements are closely keyed to using the existing technology developed under NASA Contract NAS8-25847 with MSFC. The system parameters have been updated several times during the course of this contract to reflect current JSC design requirements.

The system configuration envisions placement of at least four antenna arrays approximately 10.68 inches in diameter mounted on the spacecraft as shown in Figure 2-1.

A basic system block diagram is shown in Figure 2-2. To minimize the interface and most easily compliment the radio systems and onboard computer, the RF and computer signals and DC power will feed this system from a central point. (A configuration alternative might use multiple-point interface for redundancy at the expense of weight, power, and cost.) The radio system interface consists of a nominal transmitter input of +29 dBm at S-band and a receive output which feeds a transponder with a noise figure less than 8 dB. As noted in Table 2-1, the receive system operates at L-band also, but with degraded noise figure and gain.

Table 2-1. System Design Parameters

Transmit frequencies	2,217.5 and 2,287.5 MHz
Transmit EIRP (on boresight)	24 dBW
Transmit EIRP (scan angles)[1]	18 dBW
Array Transmit power input	30 dBm (maximum) and 28 dBm (min.)
Receiver Frequencies - S-Band[2]	2,041.9 and 2,106.4 MHz;
L-Band	1,775.5 and 1,831.8 MHz
Receive Noise temperature[3]	600°K (design goal) and 700°K (maximum)
Receive antenna gain (on boresight)	11.5 dB
Receive antenna gain (60 degree scan)	5.5 dB
Antenna beamwidth (on boresight)	40° (nominal)
Array receive electronic gain S-Band	20 dB
Array diameter	10.68 inches (main body)
Coverage	Maximized for four arrays on a 200-inch cylinder
Array thickness (including array steering controller but not power supply)	6 inches
Weight (four-array system less cables)	50 pounds (four arrays)
DC power - one array including controller	130 watts
Steering angle commands (2)	8 bits each (maximum)
Phase variation	± 12°
Amplitude variation	± 0.7 dB
Phasing time	0.2 μsec
Normal TPS bondline temperature near faceplate in front of antenna	-185°F to +350°F
Surface curvature	Flat antenna aperture

[1] 70°x 50° elliptical scan with 70° scan along X-axis.
[2] With ± 11 MHz spread spectrum at each S-band receive frequency.
[3] Degraded performance acceptable at L-band receive frequencies.

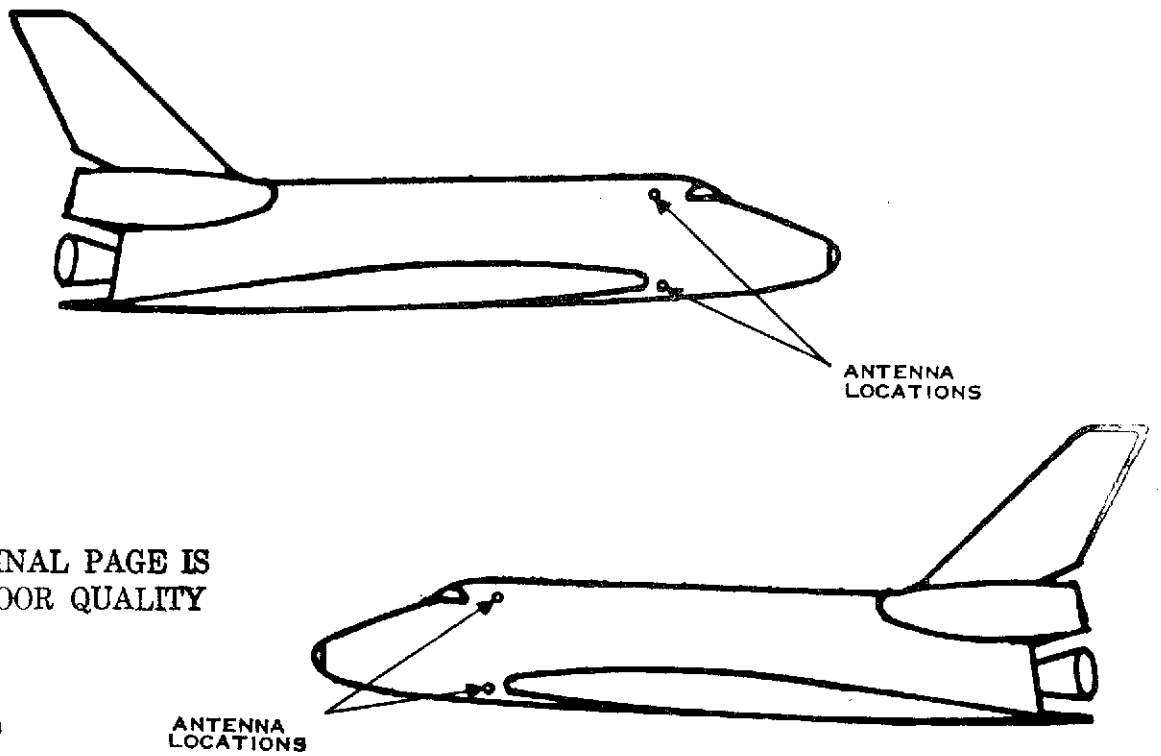


Figure 2-1. Antenna Locations

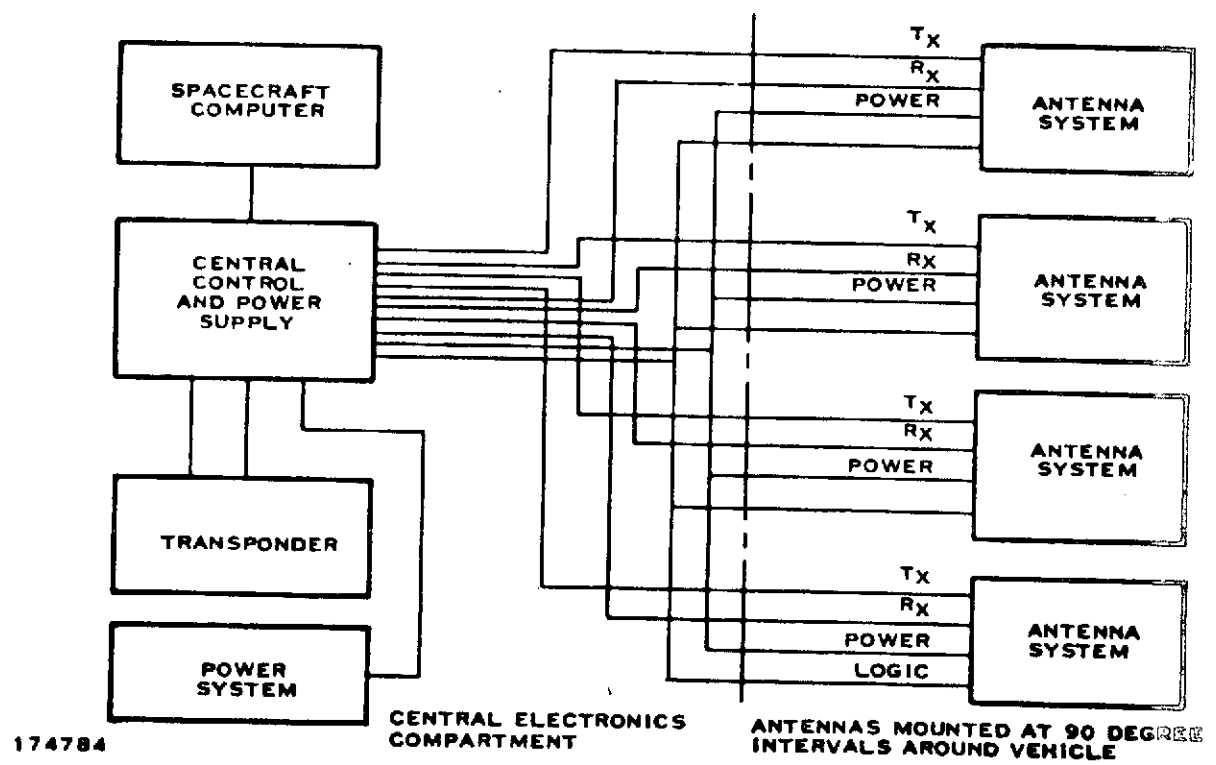


Figure 2-2. System Concept, Central Control

SECTION III

PROPOSED ARRAY SUBSYSTEM DESIGN

A. INTRODUCTION

From the general design requirements discussed in Section II, a detailed system design was completed taking into account all design trade-offs including size, weight, array location, DC power budget, and electrical performance specifications. As is usually true with most system requirements, some system parameters are in conflict with each other and a general compromise must be made to arrive at a best solution.

A drawing of the proposed communication system block diagram is shown in Figure 3-1. The commercial power supplies and central test controller are used for the breadboard array tests only. The S-Band Network Equipment is the NASA S-Band transponder and four-way RF switch.

A block diagram of the proposed SPACS antenna array subsystem is shown in Figure 3-2. The array is entirely self-contained; the only inputs required are a medium level RF signal (+29 dBm), beam steering commands, DC power, and liquid cooling fluid from a central heat exchanger and fluid reservoir. The radiating aperture consists of seven square spiral antenna elements mounted in a cavity backed housing 10.68 inches in diameter. Each element is fed by a transmit/receive microelectronic module with integral 3-bit phase shifters (phasors). An outline drawing of this antenna subsystem is shown in Figure 3-3.

The transmit input signal from the vehicle cables is separated at the triplexer module and is then split equally among the seven elements in the transmit RF manifold. The transmit manifold feeds the seven T/R microelectronics modules which in turn drive the spiral antennas.

On S-band receive, the NASA signals are picked up by the spiral antennas and then are sent to the modules. The modules amplify these signals and they are combined in phase in the receive RF manifold. The manifold is connected to the triplexer which combines the receive signal back on one line with the transmit signal on the vehicle input cable.

On L-band receive, the Air Force signals are picked up by the center antenna (0 dB) omni and is filtered and routed in the center T/R module. The center T/R module is connected to the triplexer by a cable. Total loss from the 0 dB omni antenna to the vehicle array input cable is -5 dB.

An electrical block diagram of the outer T/R module is shown in Figure 3-4. The center T/R module block diagram is shown in Figure 3-5 and the triplexer module schematic is shown in Figure 3-6.

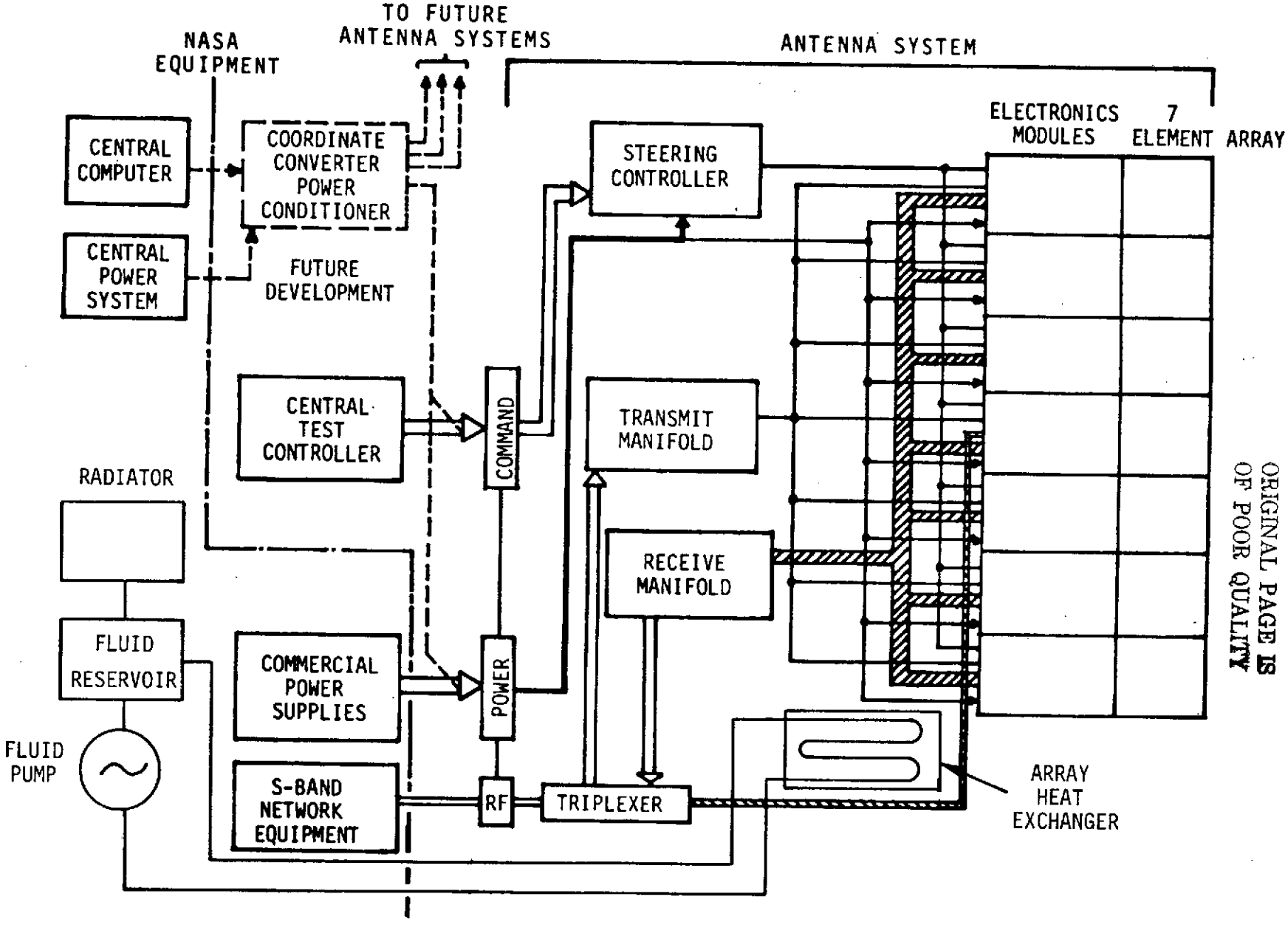


Figure 3-1. S-Band Communications System Block Diagram

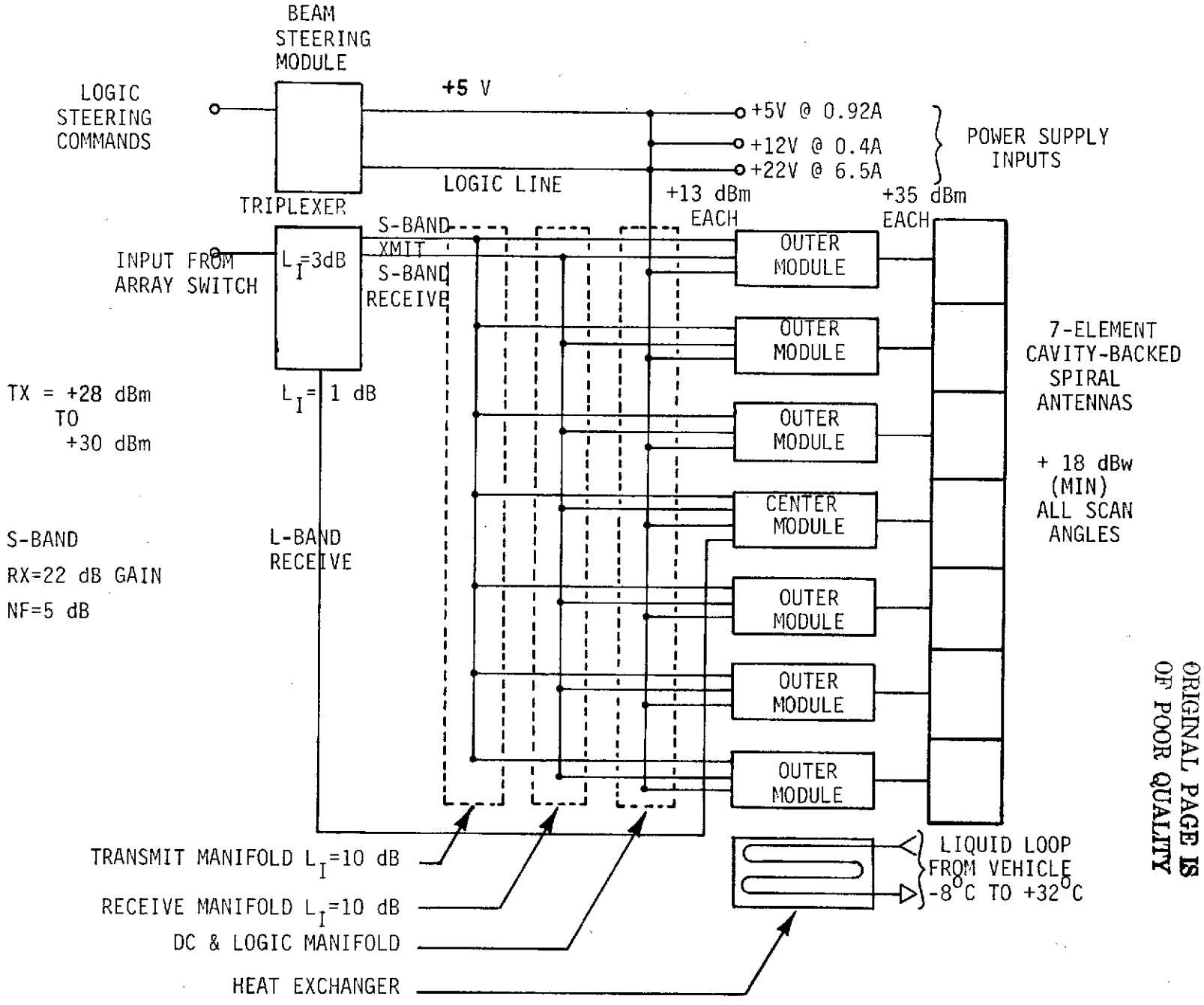
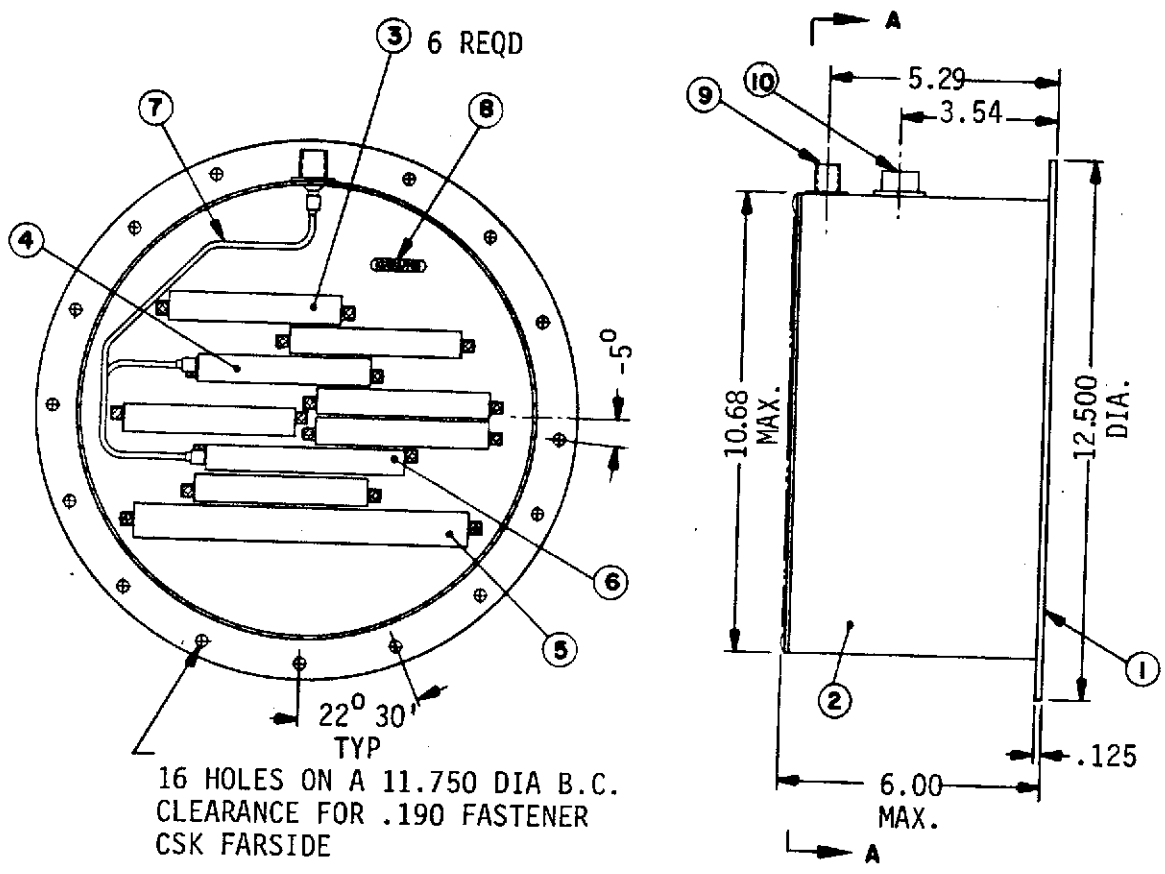


Figure 3-2. SPACS I Antenna Array Block Diagram



SECTION A-A

DESCRIPTION

1. HOUSING ARRAY
2. COVER
3. MODULE, TRANSCEIVER
4. MODULE, TRANSCEIVER, CENTER
5. LOGIC STEERING CONTROLLER
6. MODULE, TRIPLEXER
7. CABLE, SEMI-RIGID, COAXIAL
8. CONNECTOR, D.C. MANIFOLD
9. CONNECTOR, R.F. TYPE N
10. CONNECTOR, D.C.

Figure 3-3. S-Band Antenna Subsystem Outline Drawing

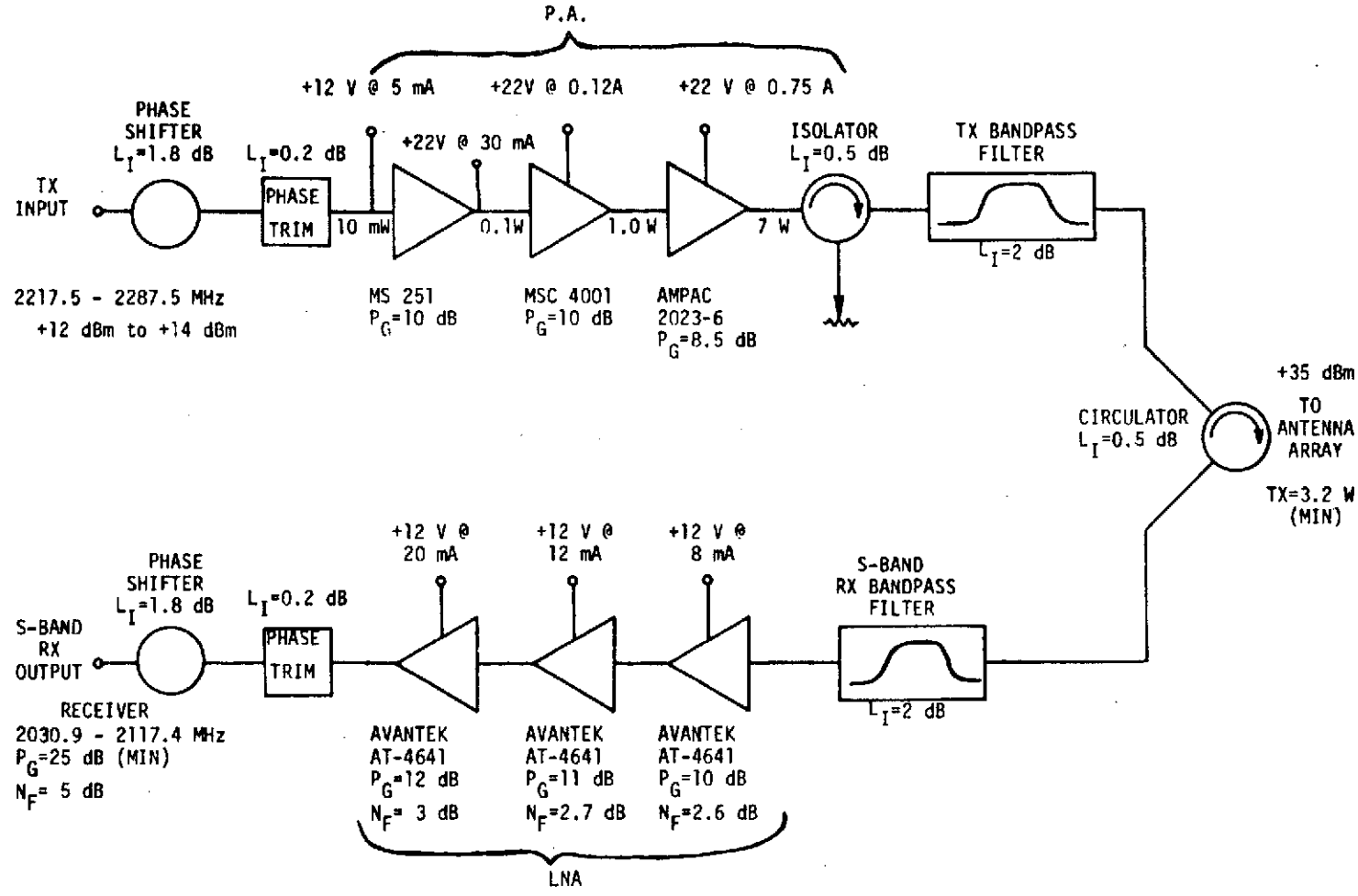


Figure 3-4. Outer Gain Module Electrical Schematic

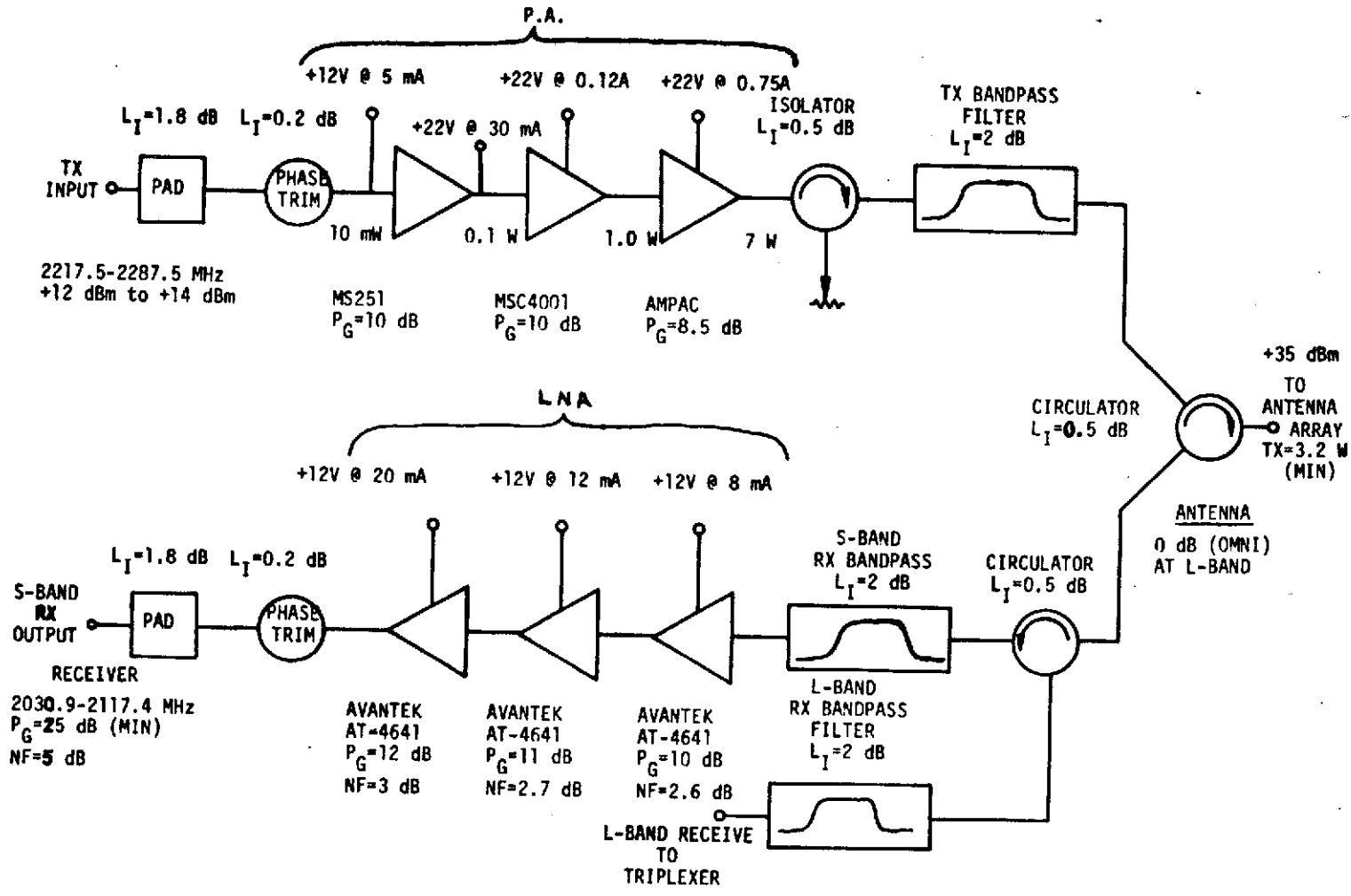


Figure 3-5. Center Gain Module Electrical Schematic

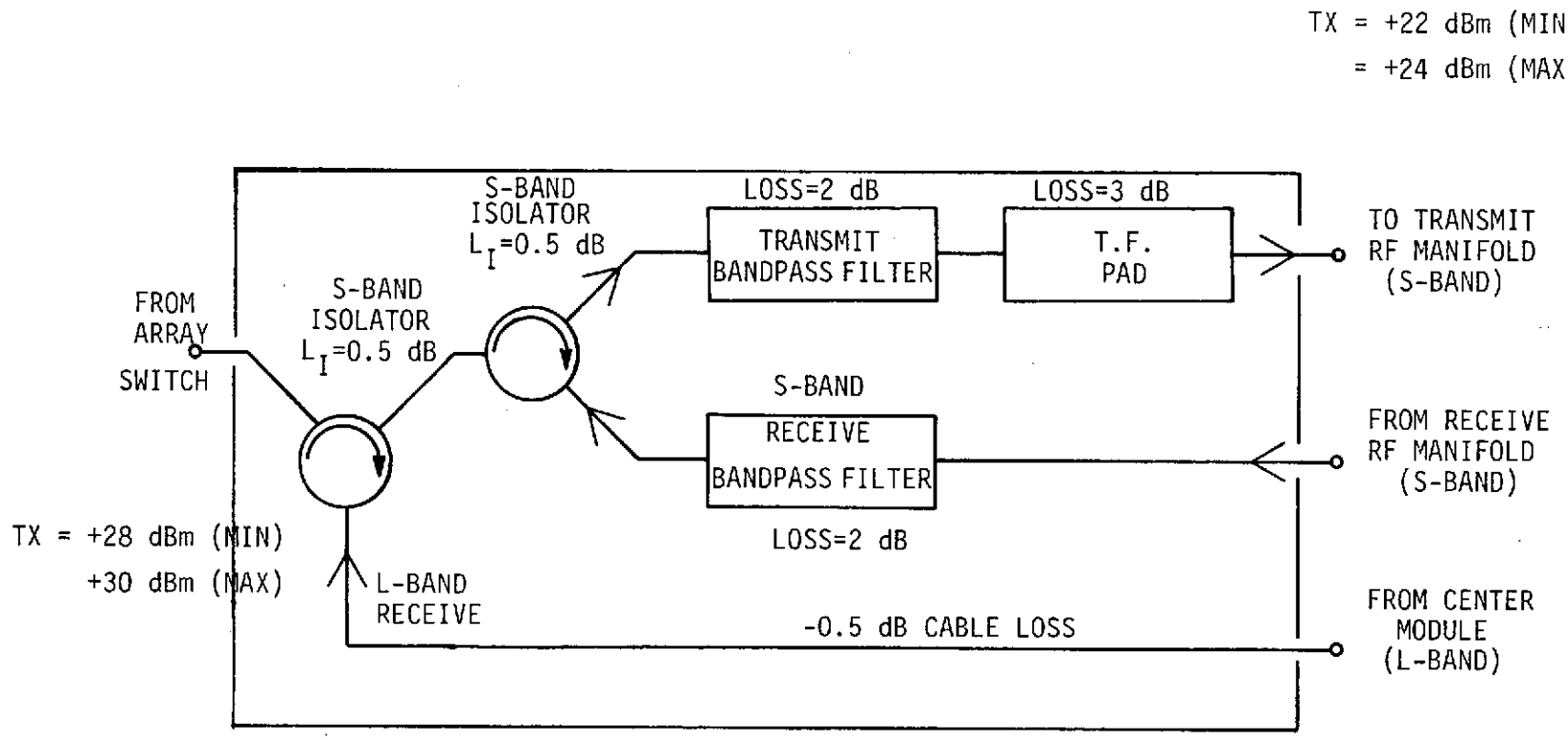


Figure 3-6. Triplexer Module Electrical Schematic

The steering (logic) controller in the antenna array calculates phase shift commands for the seven elements, to electronically steer the antenna beam in the direction commanded by the central coordinate converter unit. A DC power conditioner provides +22V, +12V and +5V array power from the regulated spacecraft DC bus.

B. SYSTEM DESIGN CONCEPTS

The detailed designs of the component parts that compose the antenna array will be discussed later in the report. Only system outlines and component specifications will be discussed under this system design section. The antenna, T/R module, RF manifolds, steering controller thermal design, mechanical design, etc., all have detailed sections that will be discussed later in this report.

Using the AESPA contract (MSFC Contract NAS8-25847), a lot of realistic component specifications had been determined from calculations and measured data. From the AESPA contract, it was determined that a seven-element active array could meet the system requirements of Table 2-1. In particular, the antenna (square spiral) elements would have the following parameters listed in Table 3-1.

Given these realistic antenna specifications, the required 18 dBW array EIRP at 70° scan angle and the seven T/R modules, the following required module power output was determined:

Transmit	18 dBW	← 70° scan EIRP
	-4.5 dB	← antenna gain
	-8.45 dB	← seven module contribution
Single Module Power Output	= 5.05 dBW = 3.2 watts	

Knowing the losses in the duplexer (0.5 dB), in the transmit filter (2 dB) to keep harmonic outputs low, and in an isolator (0.5 dB) following the final power amplifier stage to protect it from damage due to antenna mismatch, one arrives at a power amplifier output power of +8 dBW or 6.3 watts.

Since the AESPA (NAS8-25847) power amplifier already existed at approximately the same frequencies, this meant adding a matched MSC2023-6 transistor stage on the output to get a 28 dB gain power amplifier. Assuming a 2 dB loss phasor and phase trim network (a realistic number from AESPA test data), this means the T/R module would have 22 dB (min.) transmit power gain and would require a +13 dBm nominal transmit drive power to get +35 dBm (min.) output power. Thus, the transmitter side of the module was designed and is shown in Figure 3-4.

Table 3-1. Seven-Element Antenna Array Design Parameters

S-Band Transmit Frequencies	2217.5 and 2287.5 MHz
S-Band Receive Frequencies (NASA)	2041.9 and 2106.4 MHz with ±11 MHz spread spectrum at each of these frequencies
L-Band (Air Force)	1775.5 and 1831.8 MHz
S-Band Receive Antenna Array Gain (on boresight)	11.5 dB
S-Band Receive Antenna Gain (60° scan angle)	5.5 dB
S-Band Antenna Array Beamwidth (on boresight)	40° (nominal)
L-Band (single element) Receive Antenna Gain (on boresight)	0 dB
S-Band Transmit Antenna Array Gain (on boresight)	12 dB
S-Band Transmit Antenna Array Gain (70° scan angle)	4.5 dB

Maximum Diameter: 12.5 inches for antenna housing including mounting ring and 10.68 inches for main array body including dust cover.

Maximum Weight: $10^{\#}$ including RF manifolds, delrin supports, and antenna cavities.

The transmit manifold required a seven-way splitter (8.45 dB) which is hard to build easily with equal phase. Thus, an eight-way power splitter (9.03 dB), equal split-equal phase, was chosen assuming a 1 dB worst case insertion loss giving a total power divider loss of 10 dB to any one module port.

The triplexer was configured to separate the transmit/receive S-band signals. This required two filters (one for transmit and one for receive) to prevent any transmitter power leakage into the receiver (overdriving the receiver) and receiver power leakage into the transmitter forming extra transmitted beams at the receive frequencies. In addition, one circulator was required to perform the S-band (broadband) separation of transmit/receive signals and one circulator was required to perform the L-band receive combining function. Overall, this gives a 3 dB loss in the S-band side. A 3 dB pad (thin-film) is required in the transmit leg of the triplexer to adjust the transmit input signal to the module for a nominal +13 dBm drive. Without this pad, the module transmitter would be overdriven.

Now looking at the receiver, we start with the basic parameters that the array noise temperature be 600°K (design goal) and 20 dB electronic gain overall. This requires a nominal 5 dB module noise figure and 25 dB module gain. The best low noise transistors (AT-4641 by Avantek) were chosen to keep the noise figure as low as possible. This transistor is capable of about 2.3 dB noise figure with 12 dB gain. Using 3 stages in the low noise amplifier, we need about 30 dB amplifier gain and 2.8 dB amplifier noise figure.

Since the antenna input VSWR could be at least 1.8 : 1, a high Q low loss filter is required between the duplexer and low noise amplifier. The transmitter puts out +35 dBm and with a 1.8:1 antenna VSWR, this means that a maximum transmitter power of +25 dBm could be reflected back into the receiver. Since the receiver output stage (Vce = + 10V and Ic = + 20 mA) has a 1 dB compression point at +10 dBm, the receiver filter needs to have at least 45 dB rejection (loss) at the closest transmitter frequency (2217.5 GHz). The receiver filter needs to have less the 2 dB loss to keep the overall receiver noise figure less than 5.33 dB (700°K maximum noise temperature).

Again, the duplexer loss is 0.5 dB and receiver phasor loss is about 2 dB. This gives a nominal module noise figure of 5 dB and module electronic gain of at least 25.5 dB. Since the combiner loss is 1.5 dB and the triplexer S-band receive loss is 3 dB, the overall array receiver electronic gain will be at least 20 dB.

From these basic design requirements, an transmit/receive module specification was generated. The major parameters of this specification are listed in Table 3-2. A more detailed specification is given in Appendix C.

The center transmit/receive module (no phasors) requires the additional capability of L-band receive with an associated loss of 4 dB. This is to accomodate the Air Force L-band receive frequencies from the 0 dB gain central omni antenna (center square spiral element of the antenna). This is shown schematically in Figure 3-5.

From measured data on the AESPA modules, as well as numerous tests on many other Texas Instruments modules, it was determined that a maximum module case temperature range of 0°C to +45°C was required. This temperature range is required in order for the modules to meet the gain, phase, power output and noise figure parameters discussed previously.

Since the shuttle bondline temperatures vary so drastically from extreme cold values to extreme hot values, the array thermal design (to be discussed in a later section) is such that the array is thermally isolated from these bondline temperature extremes. To maintain the modules in their suitable operating range, a liquid-cooled heat exchanger will be mounted under the modules. Cooling or heating fluid will be required from the orbiter vehicle to maintain the inlet fluid temperature at -8°C to +32°C.

Table 3-2. Transmit/Receive Module Major Design Parameters

A.	Module Transmitter	
	S-Band Frequencies	2217.5 and 2287.5 MHz
	Module Power Output	+35 dBm (min.)
	Module Power Input (RF)	+13 dBm ± 1 dB
	Module Gain	22 dB (min.)
B.	Module S-Band Receiver	
	S-Band Frequencies	2041.9 and 2106.4 MHz with ±11 MHz spread spectrum at each of these frequencies
	Module Noise Figure	5 dB (nominal)
	Module Gain	25 dB (min.)
	Module Receiver 1dB Compression Point	+10 dBm Output
C.	L-Band Receive (Center Module Only)	
	L-Band Frequencies	1775.5 MHz and 1831.8 MHz
	Module Loss	4 dB (max.)
	Module Noise Temperature	440°K (max.)
D.	Module Total DC Input Power	21 watts
E.	Duplex Operation Required	

This completes the basic array design. With all these requirements and component designs, the calculated system weight and DC power budgets are shown in Tables 3-3 and 3-4, respectively. The triplexer design parameters are shown in Table 3-5 and the RF manifold design parameters are shown in Table 3-6.

Table 3-3. System Weight Budget for Proposed Flight Model

		Weight (lbs.)
A.	Four Antenna Arrays (4)	64.0
B.	Central Coordinate Converter	5.0
C.	Central Power Supply	10.5
D.	Liquid Cooling Pump & Plumbing (Central Electronics Compartment)	21.0
	TOTAL WEIGHT FOR SYSTEM	100.5 lbs.

Table 3-4. DC Power Budget For Proposed Flight Model System From 28V ± 10% Spacecraft Bus

		DC Power Budget (Watts)
A.	One Antenna Array	152.0
B.	Coordinate Converter	5.0
C.	Power Supply (80% Efficiency)	39.3
	TOTAL DC POWER FROM SPACECRAFT BUS	196.3 watts

Table 3-5. Triplexer Module Design Parameters

A.	S-Band Transmit	
	Frequencies	2217.5 and 2287.5 MHz
	Input Power	+29 dBm ± 1 dB
	Transmit Loss	6 dB
	Transmit Filter	Required
B.	S-Band Receive	
	Frequencies	2041.9 and 2106.4 MHz with ±11 MHz spread spectrum at each of the frequencies
	Maximum Input Power	+ 20 dBm
	Receive Loss	3 dB
	Receive Filter	Required
C.	L-Band Receive	
	Frequencies	1775.5 and 1831.8 MHz
	Receive Loss	1 dB including semi-rigid cable.
D.	Triplex Operation Required	

Table 3-6. RF Manifold Design Parameters (Stripline Boards)

A.	Transmit Manifold (Seven-way Split)	
	Frequencies	2217.5 and 2287.5 MHz
	Total Insertion Loss	10 dB (max.) including 7-way split
	VSWR (all ports)	1.4:1 (max.)
	Isolation (between 7 output ports)	20 dB (min.)
B.	Receive Manifold (seven-way split)	
	Frequencies	2041.9 and 2106.4 MHz with ±11 MHz spread spectrum at each of the frequencies
	Total Insertion Loss	10 dB (max.) including 7-way split
	VSWR (all ports)	1.4:1 (max.)
	Isolation (between 7 output ports)	20 dB (min.)
	Phase Matching between ports	± 5°

C. ARRAY BEAM STEERING

One set of array beam steering equations can be easily derived from basic direction cosines and referring to the array beam steering coordinate geometry shown in Figure 3-7. The general beam steering equation referred to the element phase position is

$$E = \sum_{n=1}^{N} A_n \, e^{j\,(\overline{k}\cdot\overline{R}_n - \psi_n)}$$

= array radiated power (addition of field components by summation in space)

where $\psi_n = -\beta_n$

$\overline{R}_n$ = vector between phase center and nth element

$\overline{k}$ = unit vector in direction of the target

and β_n = module element phase position.

It should be noted that several other beam steering methods are useable and equally as realizable. The advantages of the array steering equations to be described are that symmetrical element values are used and a simple sine look-up table can be used in the array (logic) steering controller.

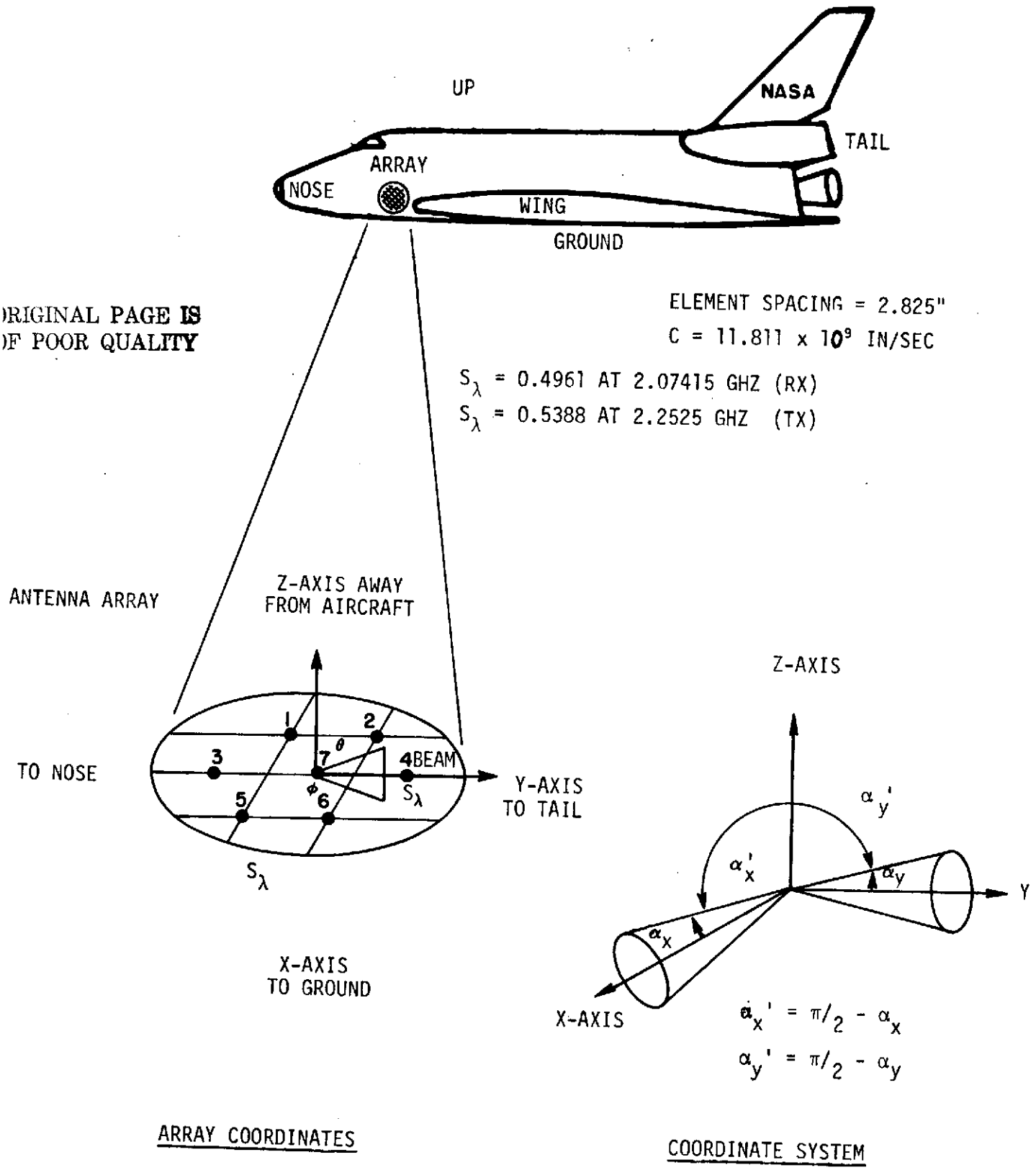


Figure 3-7. Array Beam Steering Coordinate Geometry

Using either direction cosines or a spherical coordinates we can derive the following relationships for symmetric array steering with the center element fixed at minimum phase (on boresight) position.

Let,

$$T_x = \cos \alpha_x = \cos (\pi/2 - \alpha_x') = \sin \alpha_x' = \sin\theta \cos\phi$$

$$T_y = \cos \alpha_y = \sin \alpha_y' = \sin\theta \sin \phi$$

and $$\bar{k} = k_o \left(T_x \bar{e}_x + T_y \bar{e}_y + \gamma \bar{e}_z \right) \} \bar{k} \text{ vector}$$

$$\bar{R}_6 = S_\lambda \bar{e}_x + 0.5\, S_\lambda \bar{e}_y$$

$$\bar{R}_5 = S_\lambda \bar{e}_x - 0.5\, S_\lambda \bar{e}_y$$

$$\bar{R}_2 = S_\lambda \bar{e}_x + 0.5\, S_\lambda \bar{e}_y$$

$$\bar{R}_1 = -S_\lambda \bar{e}_x - 0.5\, S_\lambda \bar{e}_y$$

$$\bar{R}_4 = S_\lambda \bar{e}_y$$

$$\bar{R}_3 = -S_\lambda \bar{e}_y$$

$$\bar{R}_7 = 0$$

$\} \bar{R}_n$ Vectors

but, $$\psi_n = \bar{k} \cdot \bar{R}_n \qquad \therefore \psi_7 = 0$$

$$\psi_1 = -2\pi\, S_\lambda \sin \alpha_x' - \pi S_\lambda \sin \alpha_y'$$

$$\psi_2 = -2\pi\, S_\lambda \sin \alpha_x' + \pi S_\lambda \sin \alpha_y'$$

$$\psi_3 = -2\pi\, S_\lambda \sin \alpha_y'$$

$$\psi_4 = 2\pi \ S_\lambda \sin \alpha_y'$$

$$\psi_5 = 2\pi \ S_\lambda \sin \alpha_x' - \pi S_\lambda \sin \alpha_y'$$

$$\psi_6 = 2\pi \ S_\lambda \sin \alpha_x' + \pi S_\lambda \sin \alpha_y'$$

The phase shift in each module or element $\beta_n = -\psi_n$

$$\beta_1 = 2\pi \ S_\lambda \sin \alpha_x' + \pi S_\lambda \sin \alpha_y'$$

$$\beta_2 = 2\pi \ S_\lambda \sin \alpha_x' - \pi S_\lambda \sin \alpha_y'$$

$$\beta_3 = 2\pi \ S_\lambda \sin \alpha_y'$$

$$\beta_4 = -2\pi \ S_\lambda \sin \alpha_y'$$

$$\beta_5 = -2\pi \ S_\lambda \sin \alpha_x' + \pi S_\lambda \sin \alpha_y'$$

$$\beta_6 = -2\pi \ S_\lambda \sin \alpha_x' - \pi S_\lambda \sin \alpha_y'$$

or using spherical coordinate references

$$\beta_1 = 2\pi \ S_\lambda \sin\theta \cos\phi + \pi S_\lambda \sin\theta \sin\phi$$

$$\beta_2 = 2\pi \ S_\lambda \sin\theta \cos\phi - \pi S_\lambda \sin\theta \sin\phi$$

$$\beta_3 = 2\pi \ S_\lambda \sin\theta \sin\phi$$

$$\beta_4 = -2\pi \ S_\lambda \sin\theta \sin\phi$$

$$\beta_5 = -2\pi \ S_\lambda \sin\theta \cos\phi + \pi S_\lambda \sin\theta \sin\phi$$

$$\beta_6 = -2\pi \ S_\lambda \sin\theta \cos\phi - \pi S_\lambda \sin\theta \sin\phi$$

$$\beta_7 = 0$$

NOTE: $\pi = 180^\circ$

Since there are only a finite number of phase positions in the 3-bit phase-shifter selected for the module, either roundoff or truncation algorithms must be used to arrive at the best phase shifter settings. From previous work, it was determined that a roundoff algorithm produces the least quantization losses in radiated power. This roundoff algorithm is

$$\Phi_N = \begin{matrix}\text{actual} \\ \text{phase shifter} \\ \text{setting}\end{matrix} = \left[\frac{\beta_A}{360^\circ} \times 2^n + 0.5\right] \frac{360^\circ}{2^n}$$

where n = number of bits in phase shifter

and β_A = calculated phase shifter setting.

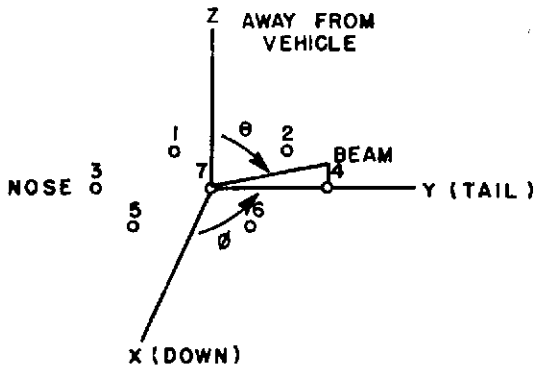
For a three-bit phase shifter this equation reduces to

$$\Phi_A = \underbrace{\left[\frac{\beta_A}{45} + 0.5\right]}_{\text{roundoff function}} \times 45^\circ$$

The roundoff occurs for the value in brackets and this bracketed value is rounded-off to the nearest whole integer.

Using the previously described beam steering equations and the round-off algorithm, we will run through two examples of beam steering in the principle planes.

Example 1:



Scan array 70° toward the tail at 2.2525 GHz with transmit phasors.

For this transmit beam,

$\Theta = 70^{\circ}$ $\quad$ $\alpha_x' = 0$

$\phi = 90^{\circ}$ $\quad$ $\alpha_y' = 70^{\circ}$

spherical coordinates $\quad$ rectangular coordinates

Then,

$$T_x = \sin\Theta \cos\phi$$

$$= \sin 70^{\circ} \cos 90^{\circ} = 0$$

using previously derived equations,

$$T_y = \sin\Theta \sin\phi$$

$$= \sin 70^{\circ} \sin 90^{\circ} = 0.94$$

or, $\beta_1 = (180^{\circ})\ (0.5388)\ (0.94) = 91.165^{\circ}$

$\ast\rightarrow \boxed{\Phi_1 \simeq 90^{\circ}}$ round-off algorithm

$\beta_2 = -180^{\circ}\ (0.5388)\ (0.94) = -91.165^{\circ}$

$\ast\rightarrow \boxed{\Phi_2 \simeq -90^{\circ}}$ round-off algorithm

$\beta_3 = (360^{\circ})\ (0.5388)\ (0.94) = 182.33^{\circ}$

$\ast\rightarrow \boxed{\Phi_3 \simeq 180^{\circ}}$ round-off algorithm

$\beta_4 = (-360^{\circ})\ (0.5388)\ (0.94) = -182.33^{\circ}$

$\ast\rightarrow \boxed{\Phi_4 \simeq -180^{\circ}}$ or set phase shifter to $+180^{\circ}$

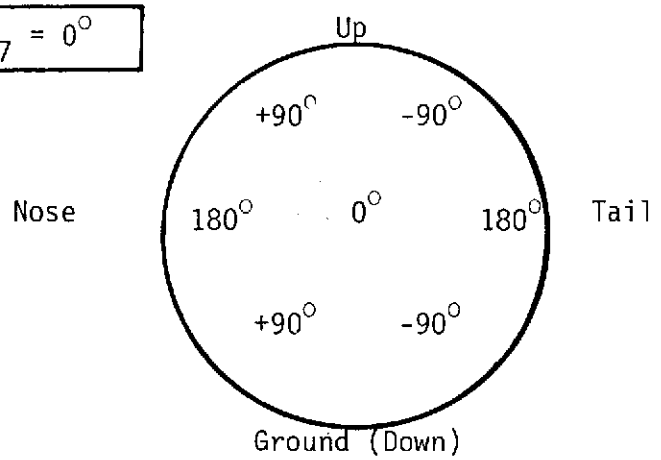
$\beta_5 = (180^\circ)\ (0.5388)\ (0.94) = 91.165^\circ$

* → $\Phi_5 \simeq 90^\circ$ round-off algorithm

$\beta_6 = (-180^\circ)\ (0.5388)\ (0.94) = -91.165^\circ$

* → $\Phi_6 \simeq -90^\circ$ round-off algorithm

* → $\Phi_7 = 0^\circ$



Module Phase Shifter Settings

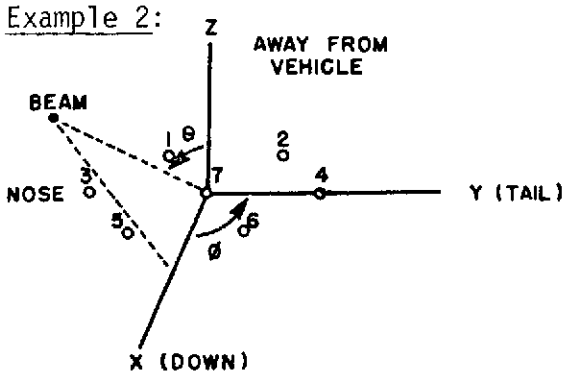
NOTE: + angles are leading

\- angles are lagging

The module phase shifters will be set so that the minimum phase length is set up for the 180° element. With reference to this minimum phase value, the $+90^\circ$ elements will have 90° more phase shift, the 0° element will have 180° more phase shift, the -90° elements will have 270° more phase shift and the -180° element will again be set to the same as $+180^\circ$ (minimum phase length).

Consider array steering like group velocity of waves. The array beam will always steer toward lagging phase side of the array.

Example 2:



Scan array 50° down to the ground at 2.07415 GHz with receive phasors.

For this receive beam,

$\Theta = 50^{\circ}$ } spherical coordinates

$\phi = 0^{\circ}$ }

or $\alpha_x' = 50^{\circ}$, $\alpha_y' = 0^{\circ}$ rectangular coordinates

Then,

$T_x = \sin \alpha_x' = \sin 50^{\circ} = 0.77$

$T_y = \sin \alpha_y' = \sin 0^{\circ} = 0$

Using previously derived equations

or $\beta_1 = (360^{\circ})\ (0.4961)\ (0.77) = 137.52^{\circ}$

→ $\Phi_1 \simeq 135^{\circ}$ round-off algorithm

$\beta_2 = (360^{\circ})\ (0.4961)\ (0.77) = 137.52^{\circ}$

→ $\Phi_2 \simeq 135^{\circ}$ round-off algorithm

→ $\Phi_3 = 0^{\circ}$

→ $\Phi_4 = 0^{\circ}$

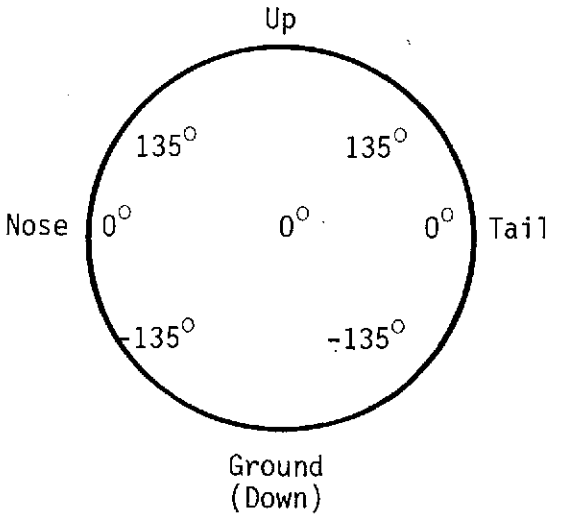
$\beta_5 = (-360^{\circ})\ (0.4961)\ (0.77) = -137.52^{\circ}$

→ $\Phi_5 \simeq -135^{\circ}$ round-off algorithm

$\beta_6 = (-360^{\circ})\ (0.4961)\ (0.77) = -137.52^{\circ}$

→ $\Phi_6 \simeq -135^{\circ}$ round-off algorithm

→ $\Phi_7 = 0^{\circ}$



Module Phase Shifter Settings

NOTE: The antenna element numbering scheme is shown by the pictorial in Figure 3-8.

Again, for reference the $+135^{\circ}$ elements would have the shortest phase length, the 0° elements would be 135° longer in phase and the -135° elements would be 270° longer in phase compared to the $+135^{\circ}$ elements.

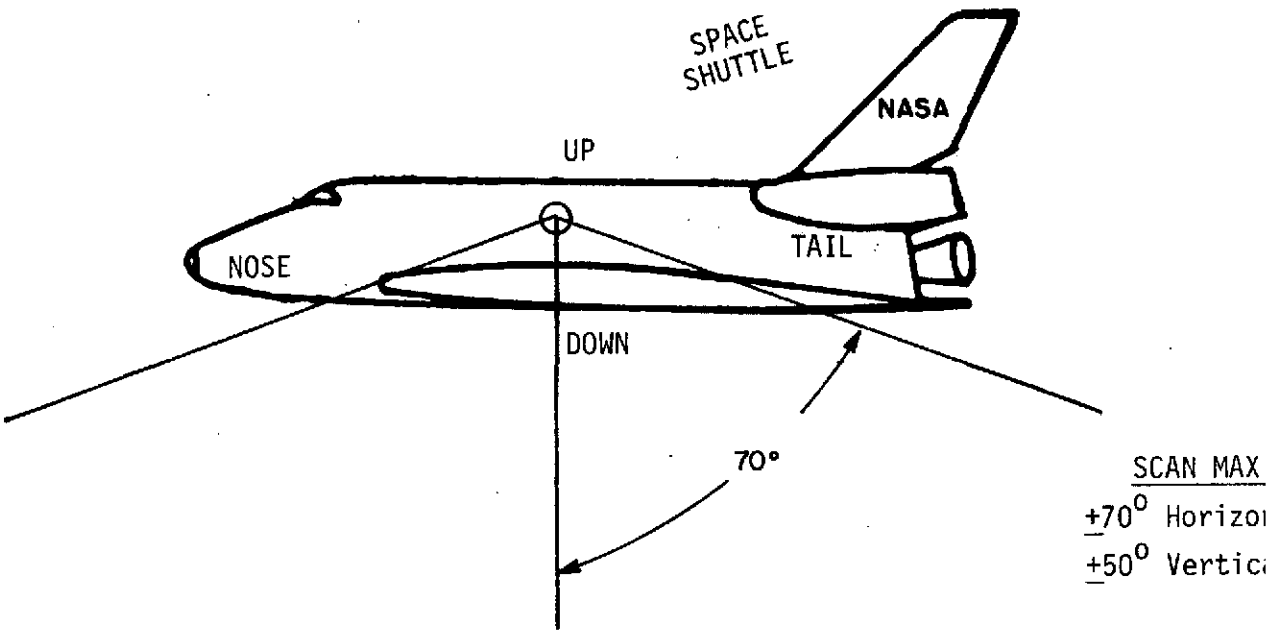
As mentioned previously, there are other array steering equations and methods available including non-symmetric element steering.

To meet SPACS I EIRP requirements and minimize quantization losses, there are only 13 optimum beam positions in the $\phi = 90^{\circ}$ plane (horizontal, nose-to-tail) and 9 optimum beam positions in the $\phi = 0^{\circ}$ plane (vertical, up and down). This only requires α_x and α_y scan angles to be 4-bits long each to produce those required beam positions.

The calculated beam positions in the two major planes are shown in Figures 3-9 and 3-10. The numbers on the horizontal axis mark the switch points for the round-off algorithm. A typical (simple) array steering logic controller is shown in Figure 3-11. This controller will be used to implement the beam steering equations described previously. It is assumed in this example that the transmitter will be pointing in a direction independent of the receiver. Read-only-memories (ROMS) are for the sine look-up tables.

D. ANTENNA ARRAY SIMULATION STUDY

A computer simulation of the array was used to calculate coverage and required computer update rate to meet all EIRP and phase requirements. To guarantee realistic values, the simulation accounted for the following degrading effects:



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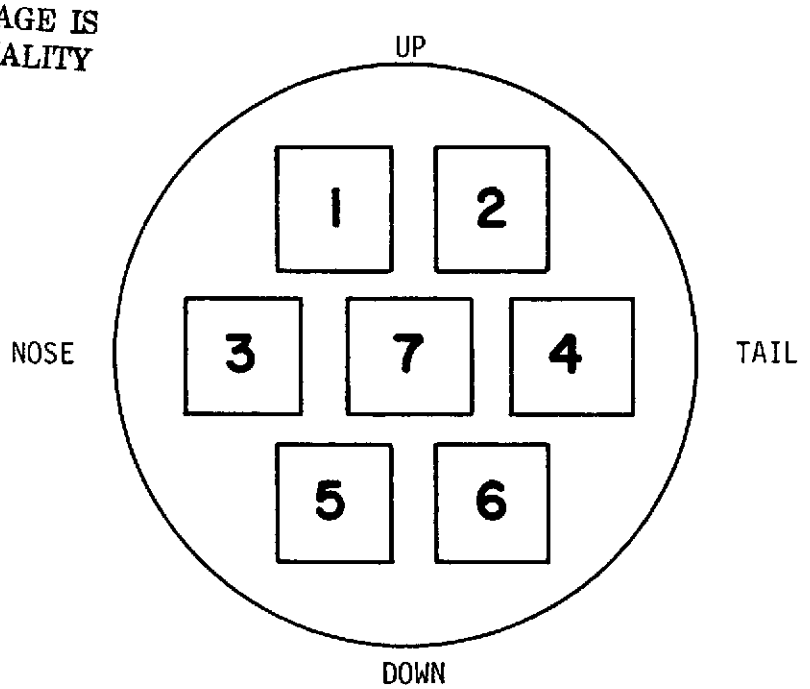


Figure 3-8. Antenna Numbering Scheme

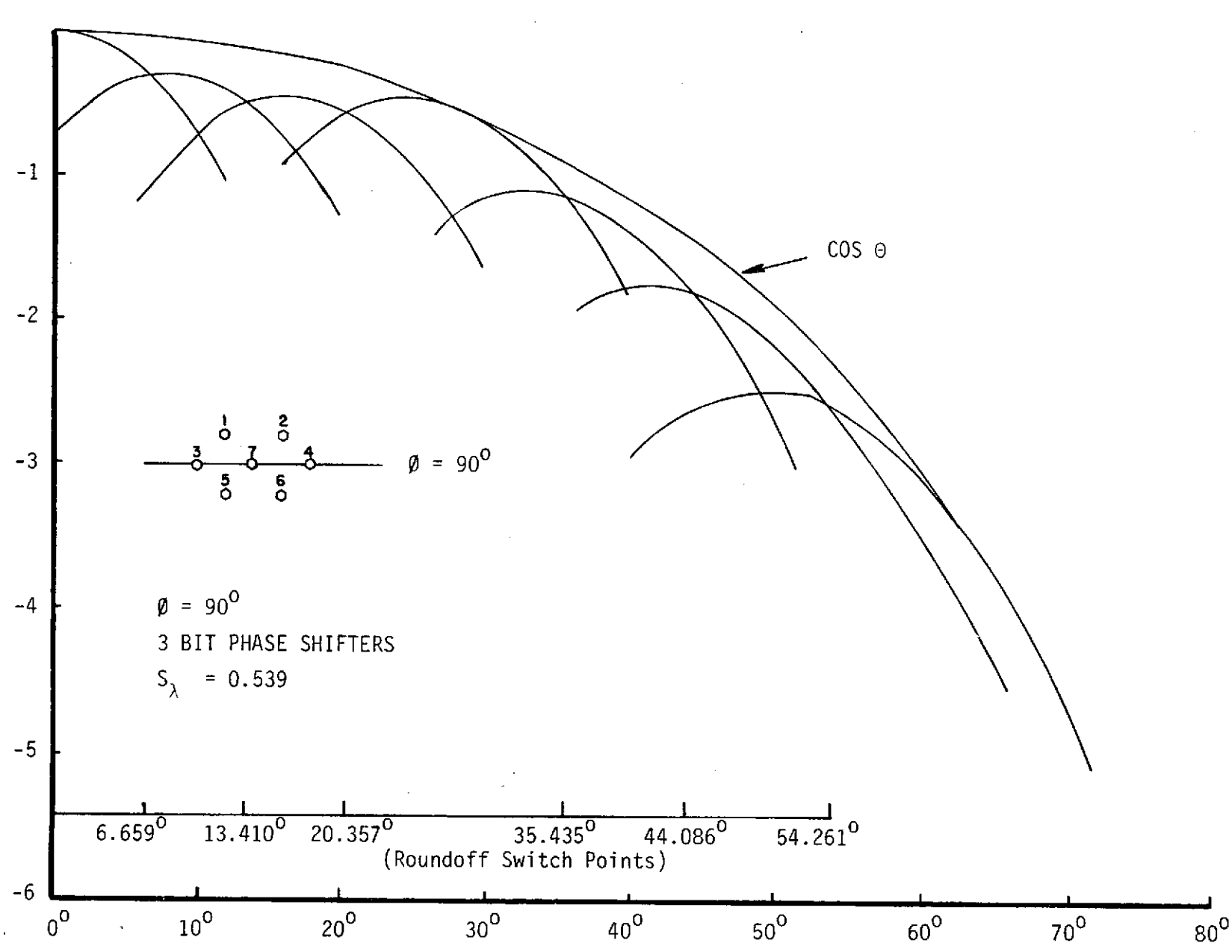


Figure 3-9. Nose to Tail (Horizontal) Antenna Scan Patterns

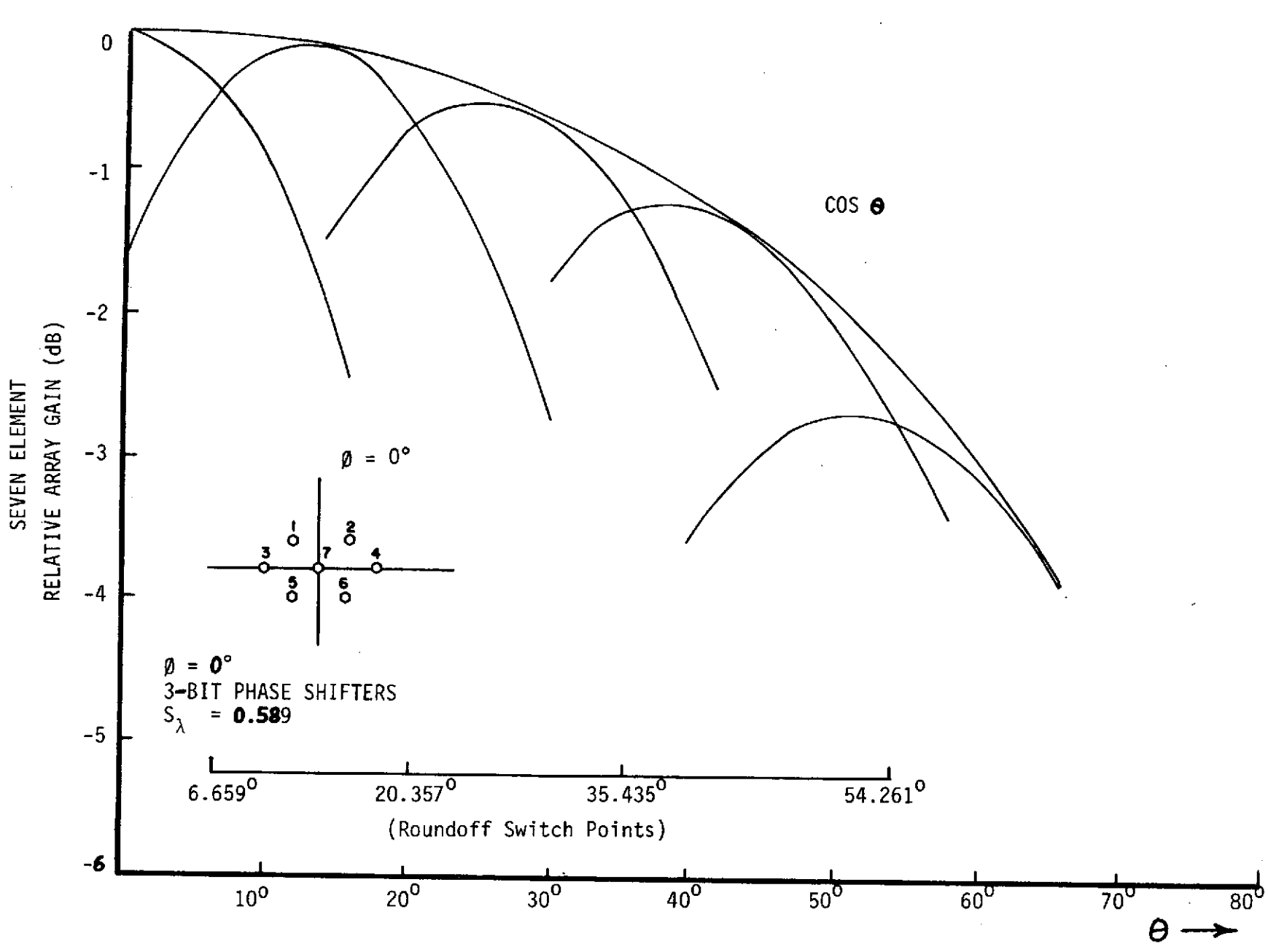


Figure 3-10. Up and Down (Vertical) Scan Patterns

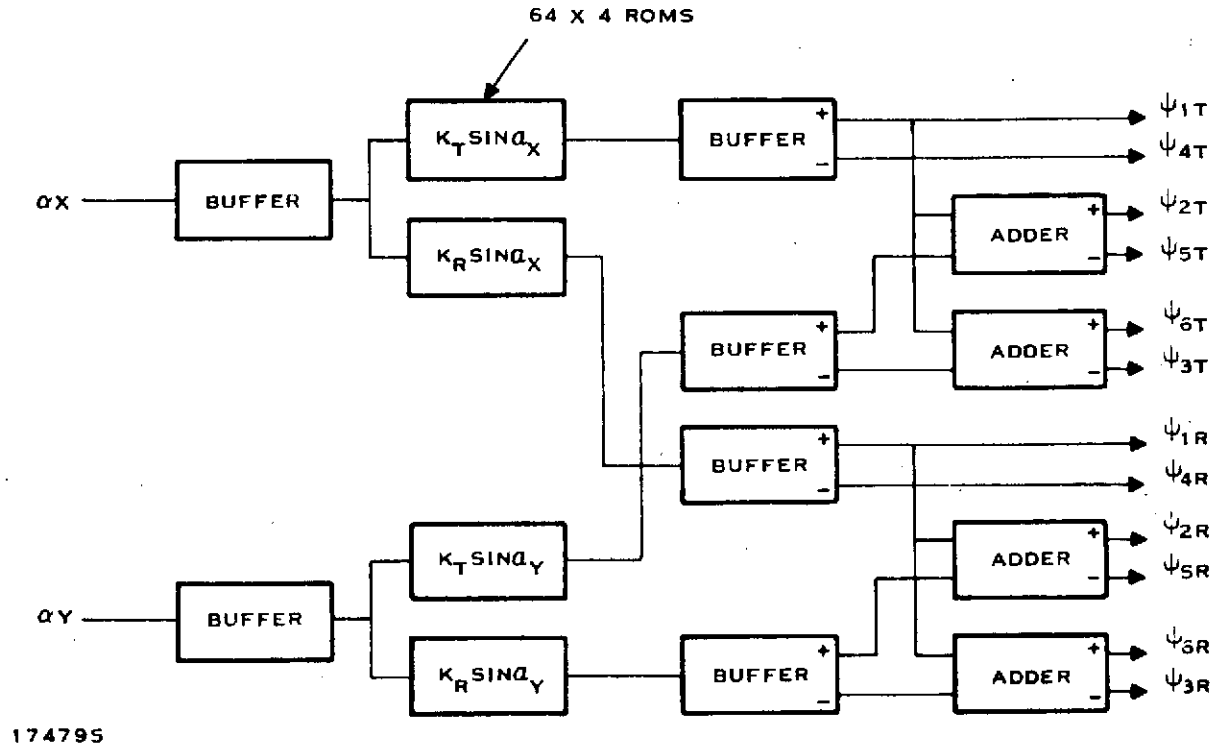


Figure 3-11. Steering Logic Block Diagram

- Radom phase and amplitude variations
- Phase quantization in phase shifter and scan controller
- Array losses
- Shuttle roll rate

This simulation was setup for the shuttle roll condition with a maximum angular motion of 20 degrees per second. The nominal combined angular motion of the shuttle is 5 degrees per sec. so the steering simulation will be for worst case conditions. Note, idealized error-free calculations would yield higher values of EIRP, but would not represent realizable coverage.

The following assumptions were made for this simulation. Phase variation of $\pm 12^{\circ}$ and amplitude variation of $\pm$ 0.7 dB due to phase and amplitude modulation from power supply ripple and noise contributions. Also included in these phase numbers are worst case phase transients induced by the switching of phasors. The resultant phase swing for a seven-element array between adjacent phase position is less than $\pm 10^{\circ}$.

Also assumed under this simulation was a center frequency on transmit of 2252.5 MHz. The results of this simulation are shown in Table 3-7. Each module was assumed to have 3.2 watts output power and the transmit antenna gain = 3.55 dB which is much worse than the 70° scan numbers actually measured for the array. A round-off algorithm was used for phasor commands.

The maximum and minimum EIRP shown in Table 3-7, lines 15 and 16, should be corrected by substracting 30 dB to give dBw EIRP values corresponding to SPACS data.

To determine the computer minimum update rate, one must look at lines 8 and 17. Setting 0.5 dB as the maximum decrease in EIRP due to computer update rate, one finds that a computer update rate of 140 msec. is required to maintain EIRP requirements. A similar simulation was done for α_x and α_y words of 4-bit length, and the same results were obtained. This is partially shown for run # 7, table width of 4 bits. Again, this minimum update rate is for 20° per second angular motion.

E. DC MANIFOLD CONCEPTS

The DC manifold will be a 12 to 15 layer fiberglass (kapton) multilayer printed circuit board. The purpose of the DC manifold is to take input DC power and logic signals from the array central DC and logic connector and distribute these signals appropriately to the array steering (logic) controller and the seven T/R modules.

Table 3-7. SPACS I Array Simulation for Seven Elements

LINE NO.	PARAMETER	UNITS	RUN # 1	2	3	4	5	6	7
1.	Elevation Command Θ_T	Degrees	45	45	45	45	45	45	45
2.	Elevation Field Point Θ_B	Degrees	45	45	45	45	45	45	45
3.	Azimuth Gommand ϕ_T	Degrees	0	0	0	0	0	0	0
4.	Azimuth Field Point ϕ_B	Degrees	0	0	0	0	0	0	0
5.	Roundoff		✓	✓	✓	✓	✓	✓	✓
6.	Updates/Revolution								
7.	Angle Between Updates	Degrees	22.5	11.25	5.02	2.81	1.41	0.70	22.5
8.	Time Between Updates	Seconds	1.125	0.563	0.281	0.141	0.070	0.035	1.125
9.	Table Length	Bits	9	9	9	9	9	9	9
10.	Table Width	Bits	8	8	8	8	8	8	4
11.	Phasor Quantization	Bits	3	3	3	3	3	3	3
12.	10-Random Amplitude Error	dB	0.7	0.7	0.7	0.7	0.7	0.7	0.7
13.	10-Random Phase Error	Degrees	10	10	10	10	10	10	10
14.	Maximum Phasor Error	Degrees	55.7	43.9	37.1	30.3	26.8	25.2	55.7
15.	Maximum EIRP	dBm	53.6	53.8	53.9	53.9	53.9	53.9	53.7
16.	Minimum EIRP	dBm	47.0	51.2	52.5	53.0	53.1	53.2	48.8
17.	Line 15 Minus Line 16	dB	6.6	2.6	1.4	0.9	0.8	0.7	5.9
18.	Maximum Gain Step	dB	2.0	0.6	0.5	0.4	0.3	0.4	1.8
19.	Maximum Far Field Phase	Degrees	17.4	14.7	14.7	16.7	9.1	9.2	10.9
20.	Minimum Far Field Phase	Degrees	-10.7	-10.2	-10.8	-11.1	-10.0	-10.8	-21.6
21.	Line 19 Minus Line 20	Degrees	30.1	24.9	25.5	25.8	20.0	20.0	32.5
22.	Phase Step	Degrees	14.3	8.6	8.2	8.0	8.0	8.0	16.3

23. R_λ = 3.0 inches Ω = 3.3 RPM P_{el} = 3.2 watts L = 0.3 dB G_{EL} = 3.55 dB f = 2252.5 MHz

A short wiring harness (3 inches long) will connect the main array connector to the DC manifold. This connector will have at least 11 pins to bring in the proper DC power and logic command signals. The array input signals are listed as follows:

The DC power and logic signals will enter the array subsystem in a single connector having the following DC pins;

a. +22 V $\pm$ 2% at 6.5 A

b. +12 V $\pm$ 2% at 0.4 A

c. +5 V $\pm$ 5% at 0.92 A

d. Regulated return line (grounded to case of antenna modules, floating at central power supply). Total ripple on the above lines is less than 0.2%.

The same connector will have the following logic pins. All commands will be TTL compatible signals with nominal 0 to 5 volts. Each incoming line to the array will be shielded in the vehicle;

a. Transmit pitch/yaw input data (8-bit serial word)

b. Receive pitch/yaw input data (8-bit serial word)

c. Array scan enable (+5 V data gate)

d. Data clock (1 - 100 KBPS signal)

e. Element select (7-bit serial word transmitted before data).

The DC manifold is mounted next to the RF manifolds and is clamped between the heat exchanger plate and the RF manifolds with suitable spacers. The DC manifold will be 0.125 inch thick, weigh 0.9 pound including DC connectors and be approximately 10 inches in diameter. Nine DC connectors similar to the multipin connectors on the modules will be mounted on the DC manifold. One of these connectors will have 11 pins and mate to the short array connector wiring harness. One connector will have 31 pins and mate to the steering (logic) controller connector; and the other seven connectors will have 15 pins and will mate to the module connector.

This manifold will be defined further, designed, and fabricated later on the SPACS II Contract NAS9-14485. It will be a straight forward layout and MLB fabrication effort.

F. ANTENNA ARRAY LIGHTNING PROTECTION

The NASA antenna array lightning protection requirements for the Space Shuttle as defined by the "Space Shuttle Lightning Protection Criteria Document" MSC-07636, are not clearly defined for internally mounted antennas which are flush mounted to the skin. Since the SPACS I antenna would be mounted behind the thermal protection structure of the vehicle, lightning would have to first penetrate and burn a hole in the following layers before it could damage the SPACS antenna arrays. These layers are (1) 0.325 to 3.25 inch thickness of LI-900 HRSI tile, (2) 0.165 inch thickness of strain isolator pad (SIP) made of felt, (3) a honeycomb fiberglass carrier panel with a nominal thickness of 0.025 inch, and finally (4) a moisture avoidance pad (MAP) that is .015 inch to .045 inch thick.

The antenna requirements that do apply to the SPACS antenna position are (1) overall array grounding to drain off current or built up charge and (2) prevention of lightning being passed down through the center conductor of the array to the S-band transponder and hence, knocking out the S-band transponder.

The proposed SPACS system design would have the following design to meet the two previously mentioned lightning requirements. First, should lightning penetrate or burn a hole in the thermal protection system of the vehicle and strike the antenna element cavity housing, the charge or current associated would be drained away by a braided ground strap that is connected between the metal antenna cavity housing and the aluminum skin of the shuttle. Should the lightning bolt strike the spiral antenna elements themselves, the elements struck would in all reality vaporize due to the high currents involved. The thin etched patterns could not conduct away a continuous current of 400 amperes for 0.3 seconds. The lightning stroke would most likely damage only one of the seven spiral antenna elements.

Second, should the lightning stroke get on the center conductor of the antenna feed, it is prevented from damaging the T/R modules by the high Q receive combline filter and the MIC transmit filter. These two filters have built in as an integral part of the filter several large DC blocks (air gaps). In addition, the amplifiers and phasors in both the transmitter and receiver portions of the modules also have numerous DC blocking capacitors as well as 0.25 λ_g DC return lines to drain off current to ground. Finally, the triplexer module (mounted just ahead of the array input connector) has MIC filters which also act as good DC blocks to any current.

These previously mentioned design features are built into the array to minimize lightning damage to the array itself as well as prevent lightning from being transmitted down the center conductor to the transponder. It is very unlikely that lightning could damage the arrays or the S-band transponder because of these good design features.

SECTION IV

ANTENNA DESIGN AND EVALUATION

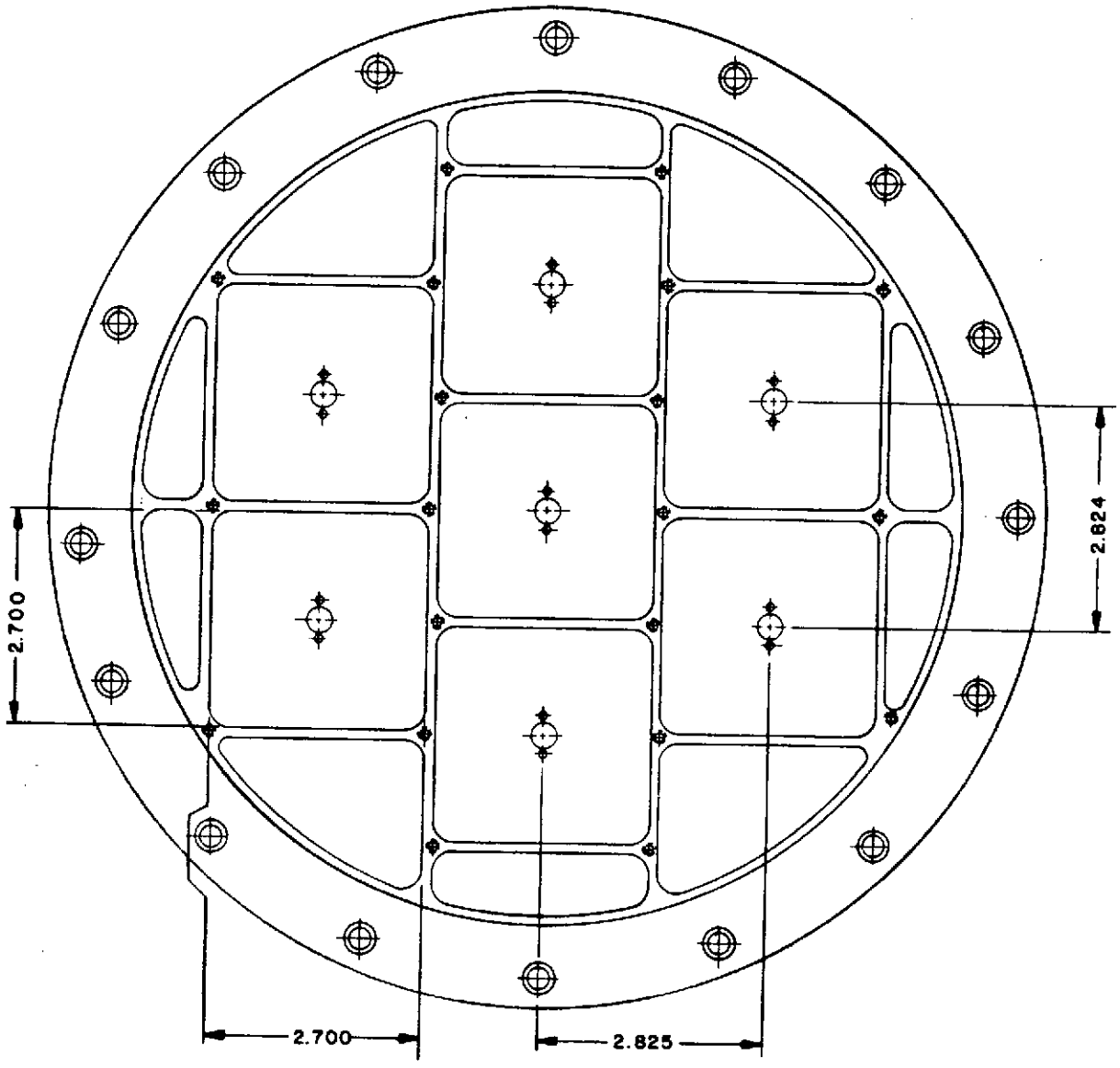
A. ANTENNA DESIGN

The SPACS I antenna is a seven-element, square spiral array arranged in a triangular grid as shown in Figure 4-1. The array grid and element size were chosen in order to make maximum use of the available aperture and hence, achieve maximum gain.

In the initial phase of this program a seven-element, square spiral array designed for operation at approximately 1600 MHz was studied experimentally. This work was documented in monthly progress report number 2. From the data it was seen that the simple balun design shown in Figure 4-2 possessed sufficient bandwidths for SPACS. This balun transforms from 50Ω into two 100Ω arms, one being 180° (at f=2.1633 GHz) longer than the other. The balun and spiral are connected using a twin coaxial line with a fiberglass card separation.

This work led to a single element study examining two cavity designs and two spiral designs. The depths of the cavities were chosen to be 0.455 in. ($\lambda/12$ at 2.16 GHz) and 0.682 in. ($\lambda/8$ at 2.16 GHz). Note that the cavity width was chosen to be 2.7 in. ($\lambda/2$ at 2.186 GHz). The first spiral was a truncated version of the L-band array spiral design. In general, this design gave unsatisfactory results due to the large separation between sprial turns. This in turn led to the new design of a spiral element which is shown in Figure 4-3. The design is self-complementary with a line width of 0.020 inch. It was found that the addition of an RF absorptive coating (Emerson-Cuming Eccoorb 268E) was quite effective in minimizing the axial ratio. This is accomplished by the reduction of reflected end currents which radiate the opposite sense circular polarization. The coating is placed on the outer five lines on the spiral. The single element patterns are shown in Figures 4-4, 4-5, and 4-6. Note that the element patterns are very similar to $\cos\theta$. Figure 4-7 illustrates the gain and axial ratio for both of the cavity depths. From this data, the data shown in Table 4-1 can be derived. On the basis of this information, the thicker cavity was chosen so that the EIRP requirements would be met at 70°.

An engineering model of the seven element array was then built. For this array, seven of the single element baluns were built and mounted on the rear of the cavity structure. Also, seven ports of an S-band, sixteen-way, power divider were used for feeding the array for a broadside pattern. Data was obtained with the array mounted in a cylindrical ground plane with rolled edges in order to minimize diffraction effects and to insure that large angle radiation will be as close as possible to the actual environment. This same ground plane was also used for the breadboard antenna. Figure 4-8 illustrates the matched circularly polarized gain of the array as a function of frequency. Note that generally the specifications are exceeded by about 1 dB. Figure 4-9 illustrates the broadside axial ratio as a function of frequency. The maximum axial ratio is approximately 2.0 dB. Figure 4-10 illustrates the input reflection coefficient of the central element from 1.7 - 2.4 GHz. The input VSWR is nominally 1.4 : 1 at the transmit frequencies.



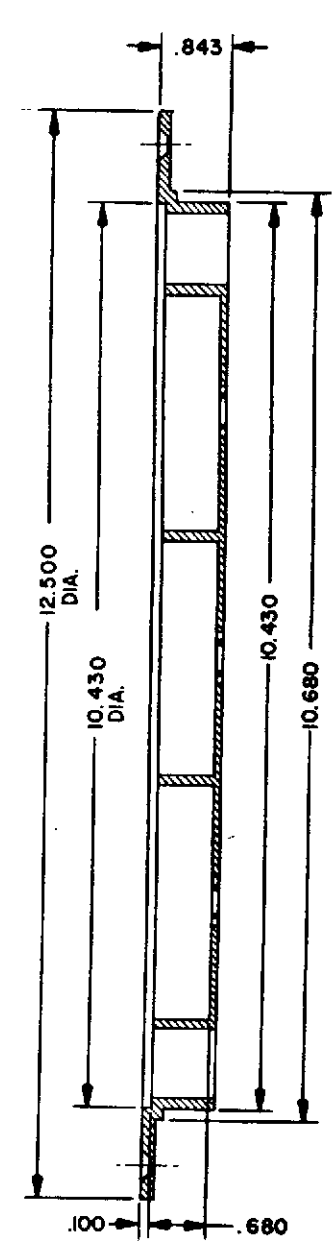


Figure 4-1. Aluminum Cavity Housing, SPACS I Antenna

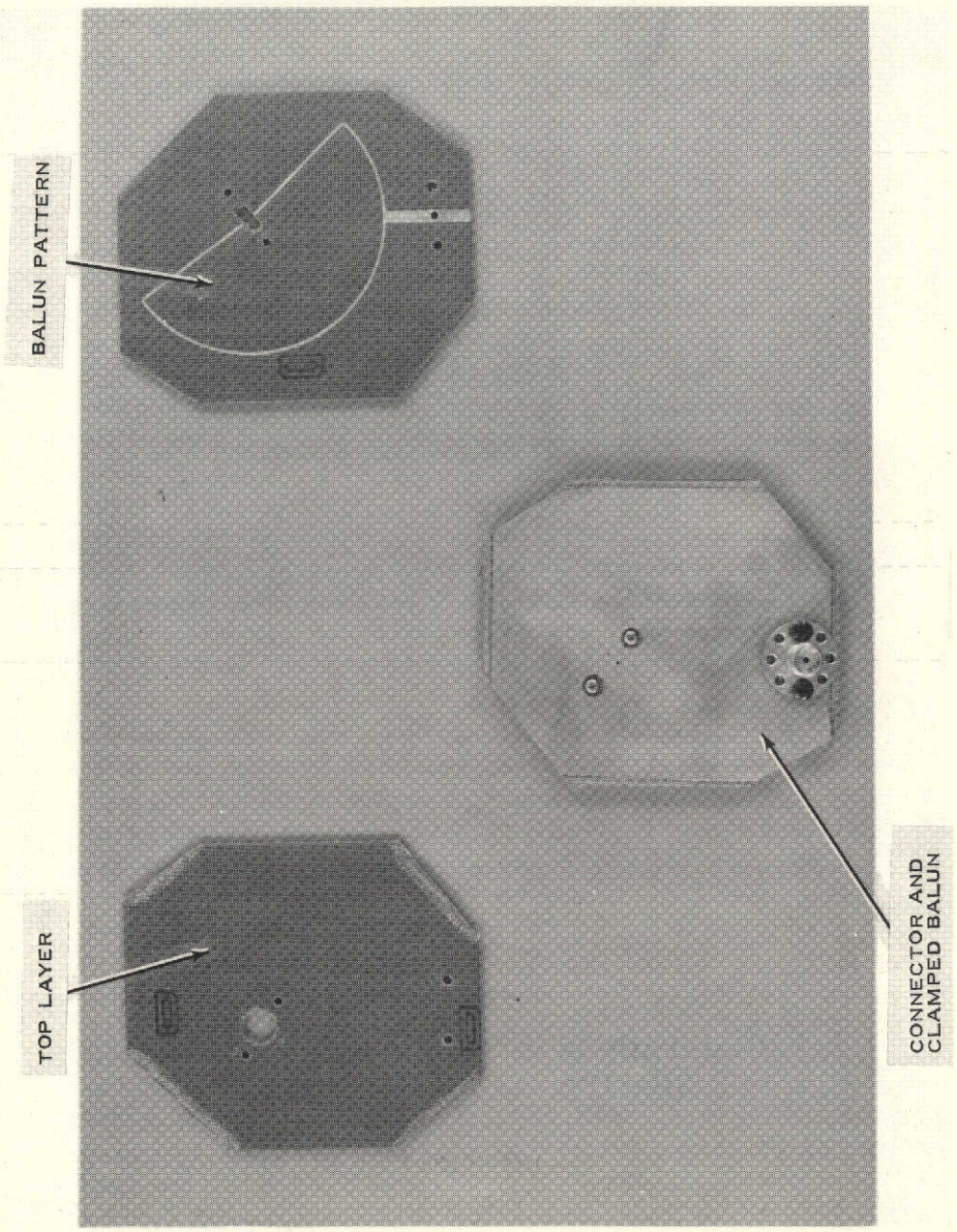


Figure 4-2. Single Balun for Engineering Evaluation

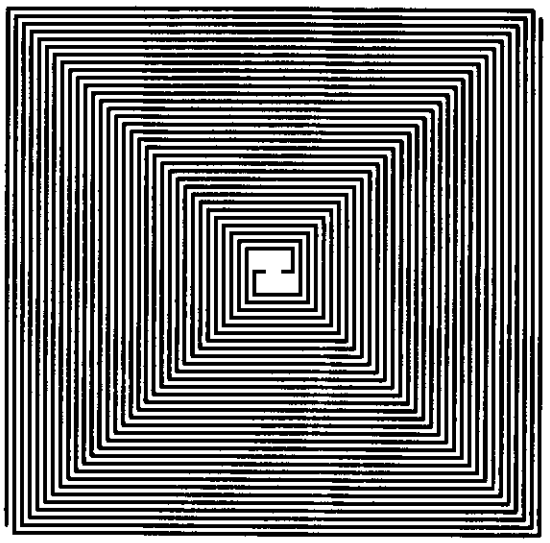


Figure 4-3. Spiral Antenna Element

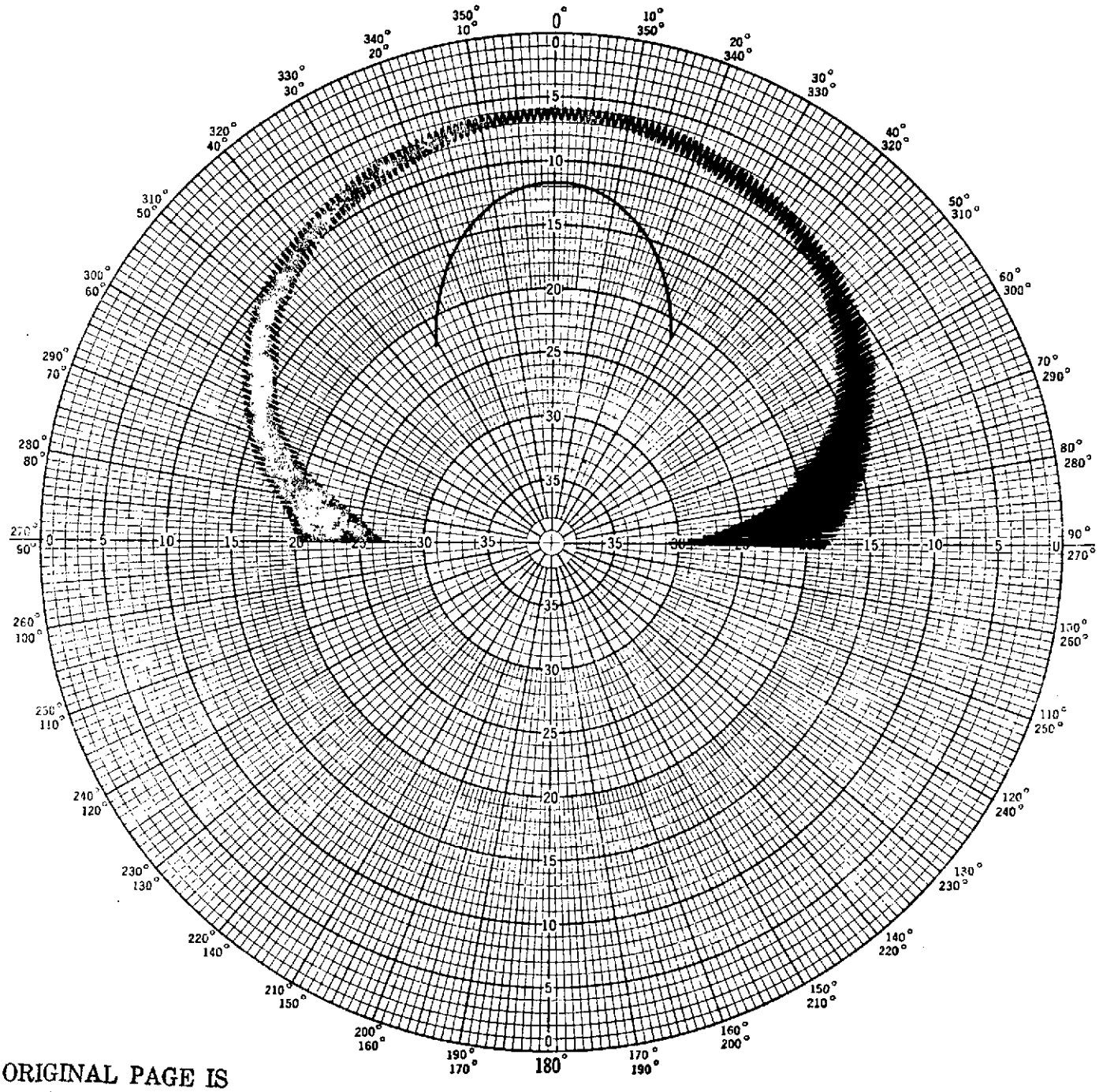


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Figure 4-4. Spiral Antenna on 0.455 Inch Cavity, 1.8 GHz

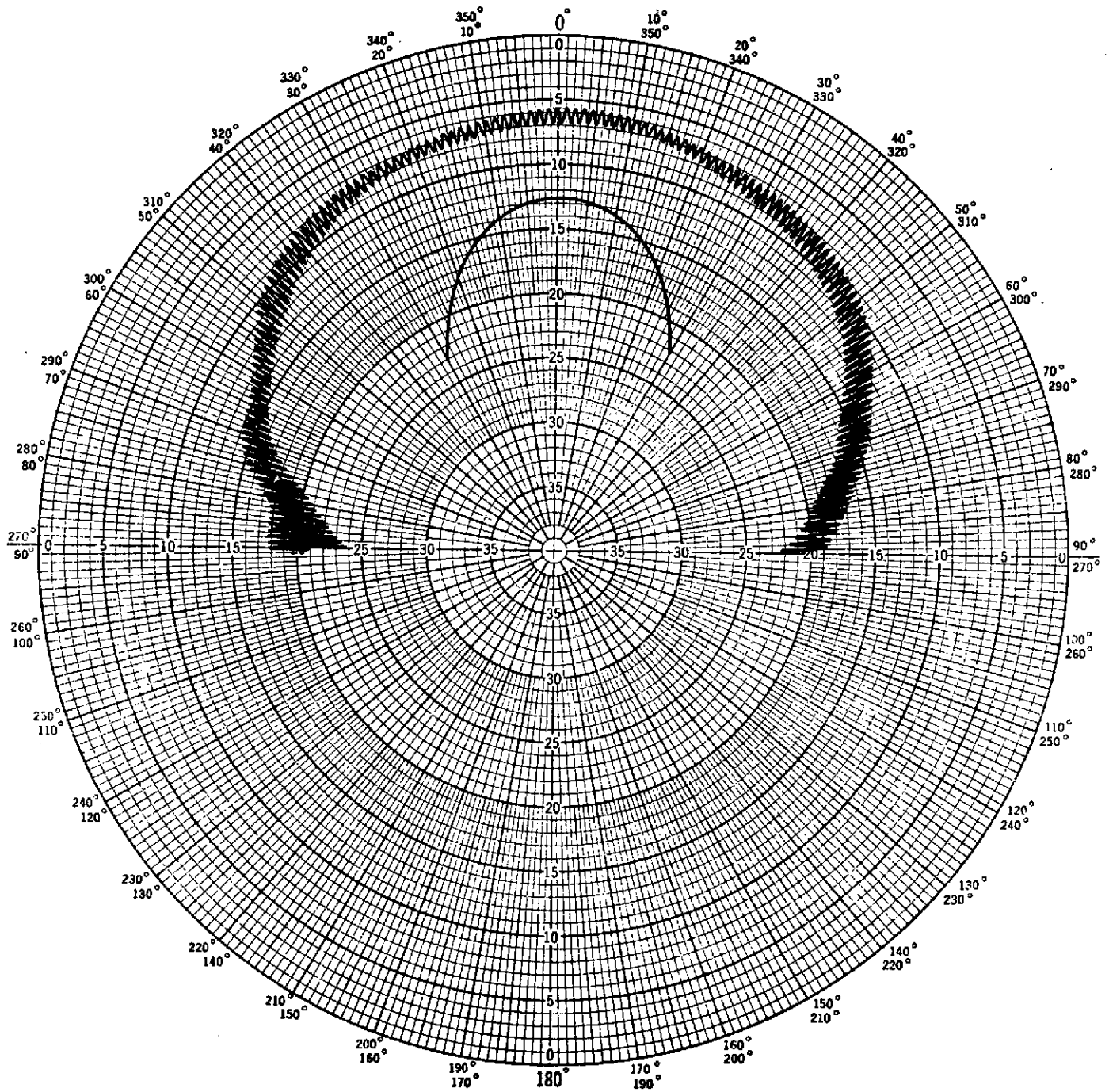

Figure 4-5. Spiral Antenna on 0.455 Inch Cavity, 2.0 GHz

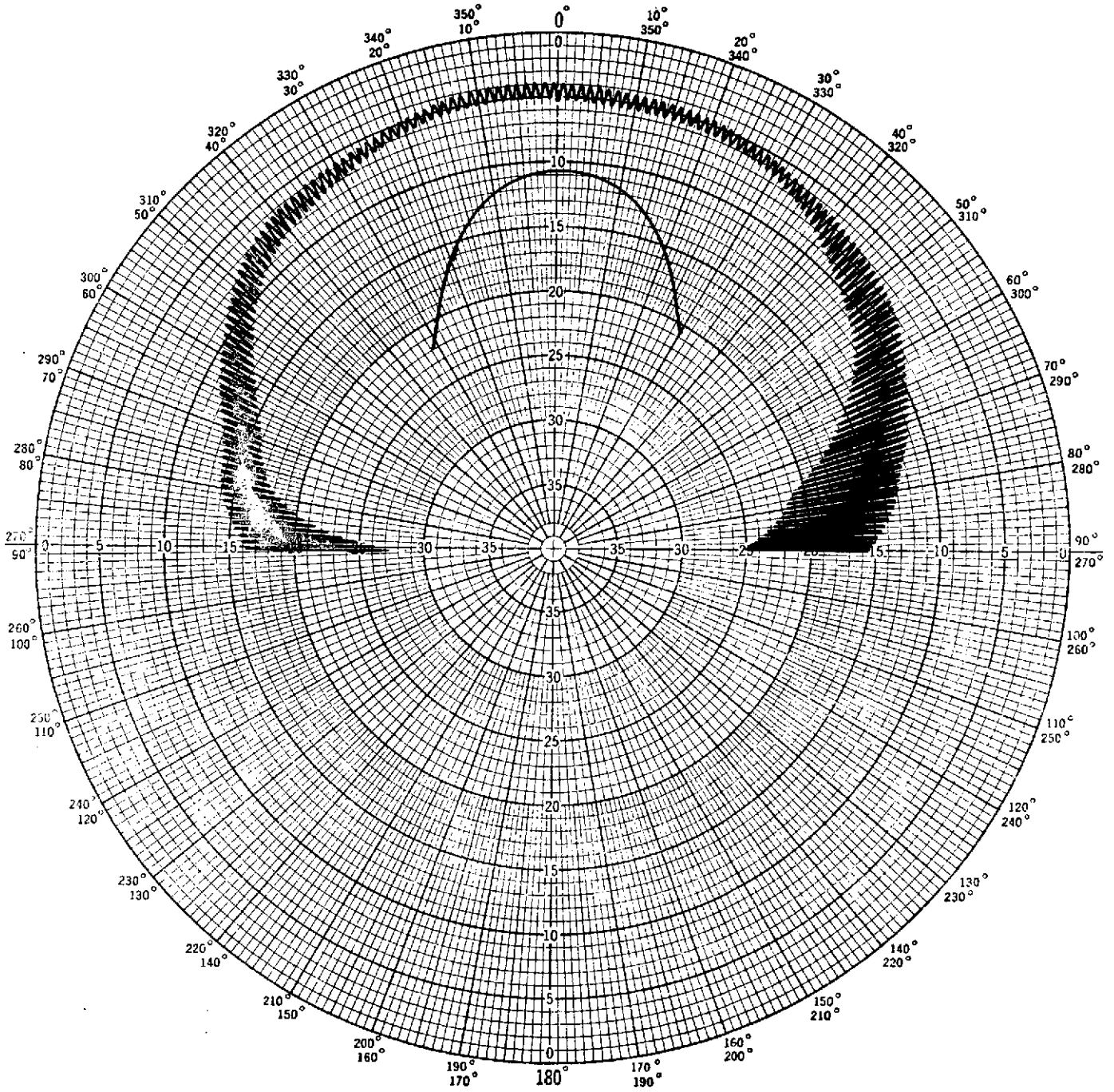

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Figure 4-6. Spiral Antenna on 0.455 Inch Cavity, 2.2 GHz

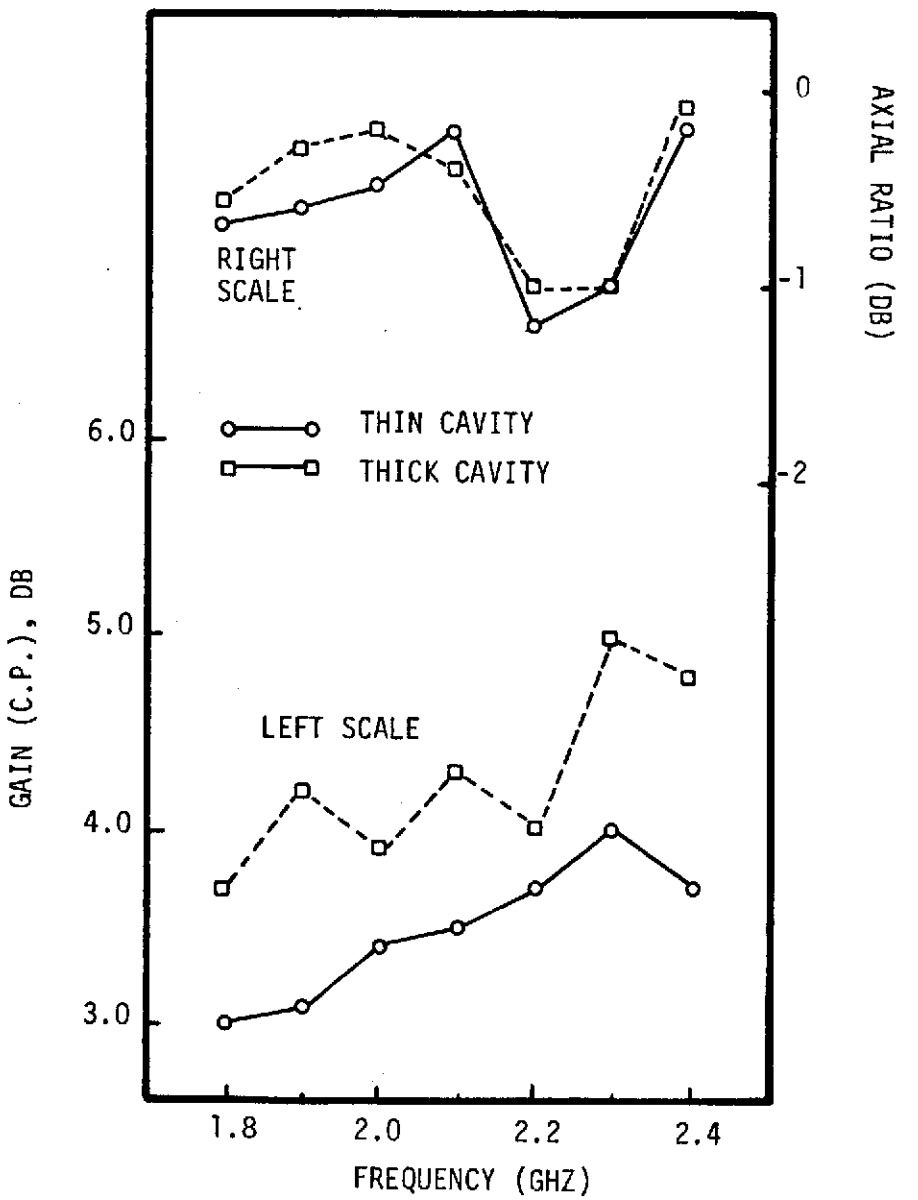

Figure 4-7. Gain and Axial Ratio Versus Frequency, S-Band Spiral Antenna

Table 4-1. Projected Array Performance Based On Single-Element Test Data, 4 Nov. 1974

PARAMETER	0.455" CAVITY		0.682" CAVITY		SYSTEM REQUIREMENT
	XMIT	RCV	XMIT	RCV	
ELEMENT GAIN					
AT Boresight	3.8 dB	3.5 dB	4.3 dB	4.1 dB	
At 50°	-0.5 dB	-0.2 dB	0.8 dB	0.6	
At 60°	-1.9 dB	-1.8 dB	-1.15	-1.5	
At 70°	-5.5 dB	-6.0 dB	-3.8 dB	-4.0 dB	
ANTENNA GAIN					
At Boresight	12.25 dB	11.95 dB	12.75 dB	12.55 dB	11.5 dB, Min.
At 50°	7.95	8.25	9.25	9.05	--
At 60°	6.55	6.65	7.30	6.95	5.5 dB, Min.
At 70°	2.95	2.45	4.65	4.45	--
EIRP					
At Boresight	25.75 dBw	--	26.25 dBw	--	24 dBw, Min.
At 50°	21.45	--	22.75	--	--
At 60°	20.05	--	20.80	--	--
At 70°	16.45 dBw	--	18.15 dBw	--	18.0 dBw, Min.

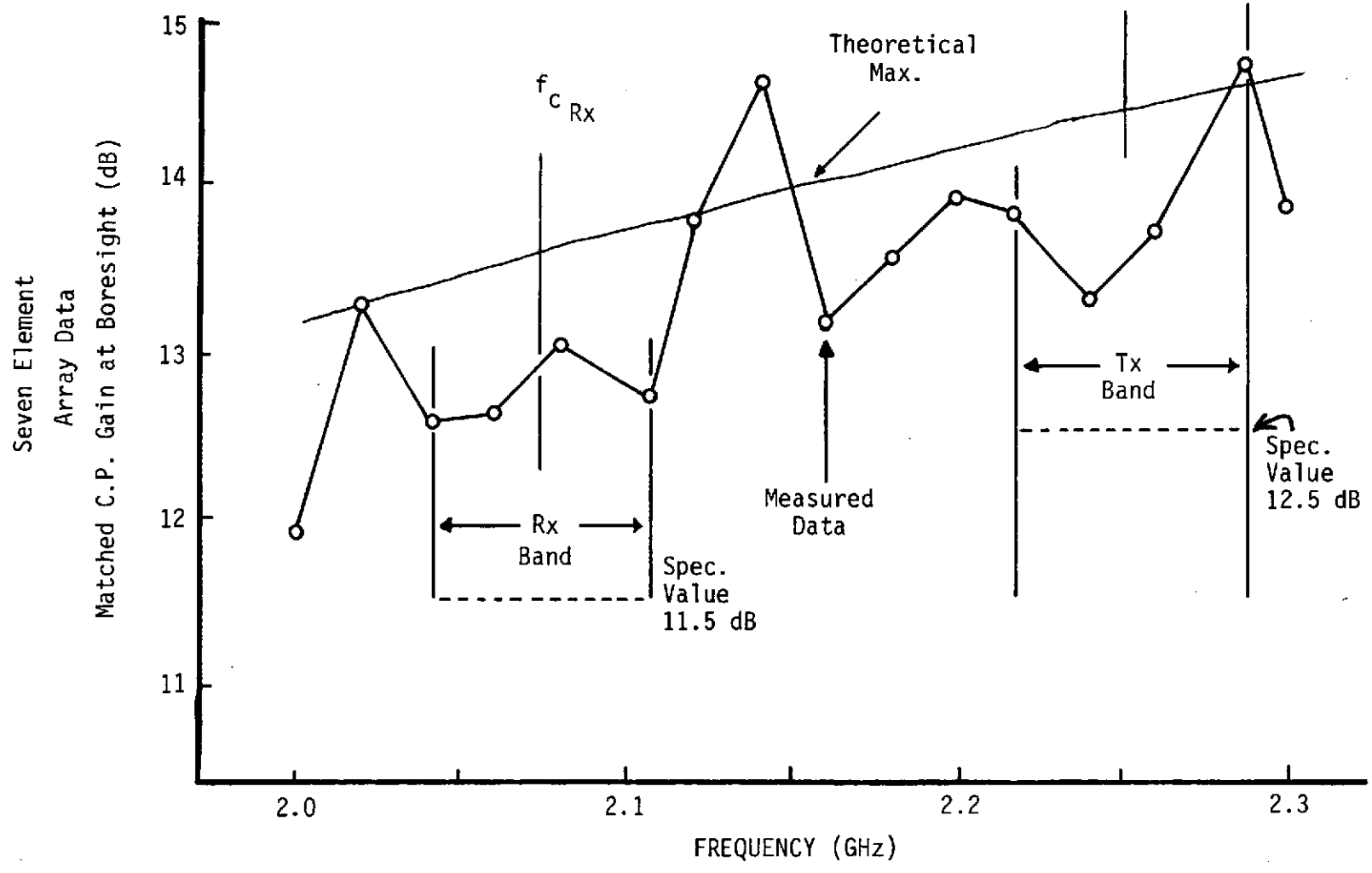

Figure 4-8. Seven Element Evaluation Antenna Array Gain

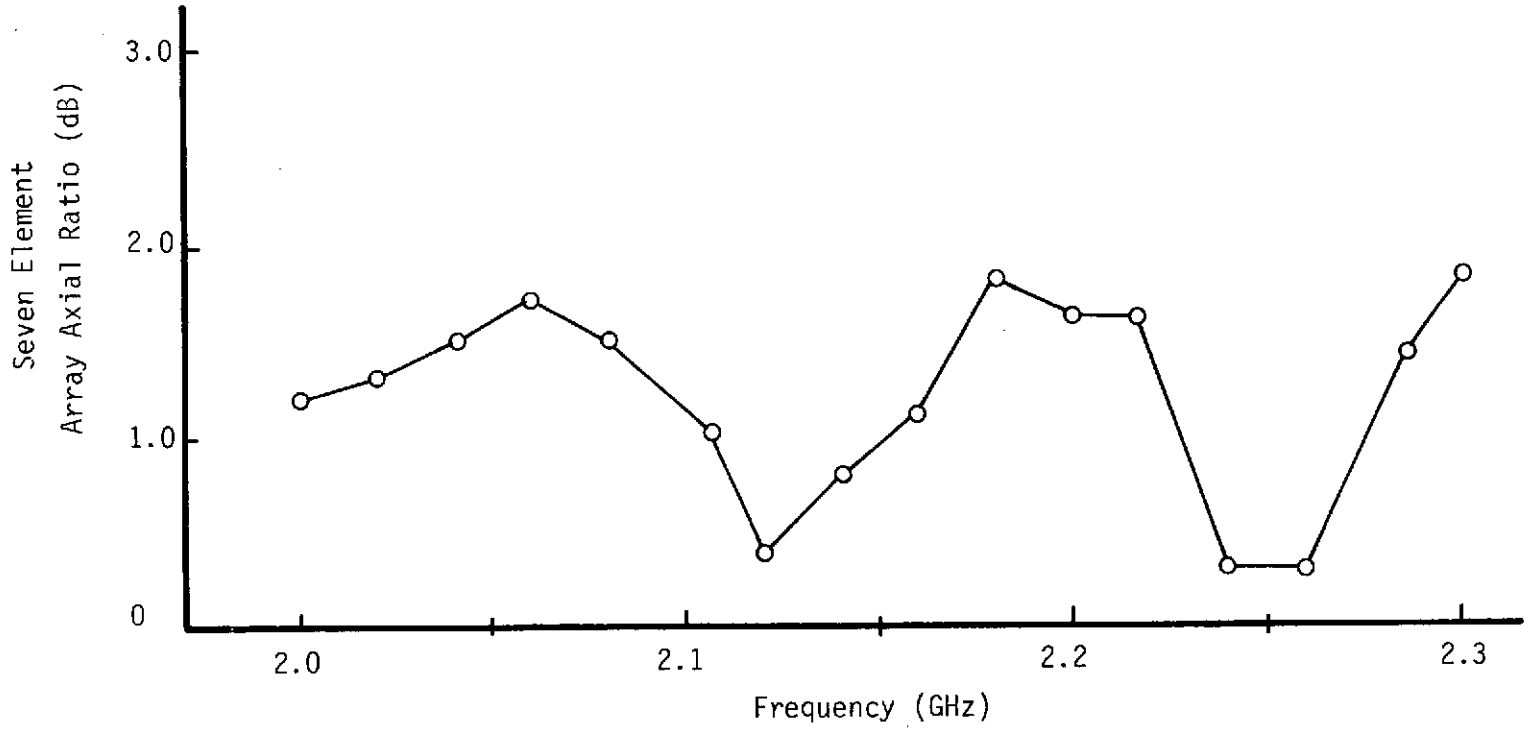

Figure 4-9. Seven Element Evaluation Antenna Array Axial Ratio

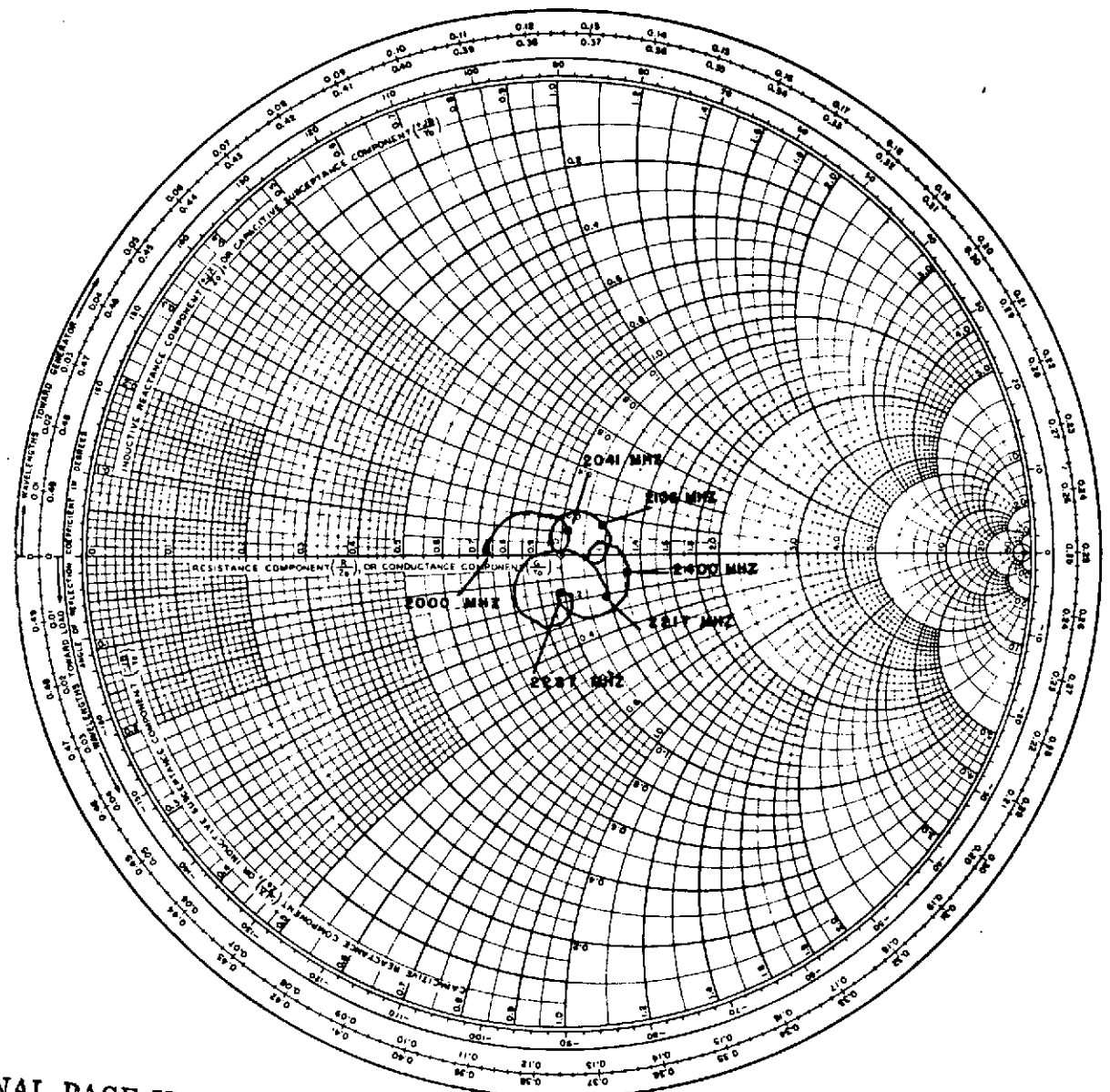

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Figure 4-10. Central Element Impedance for Engineering Evaluation Antenna

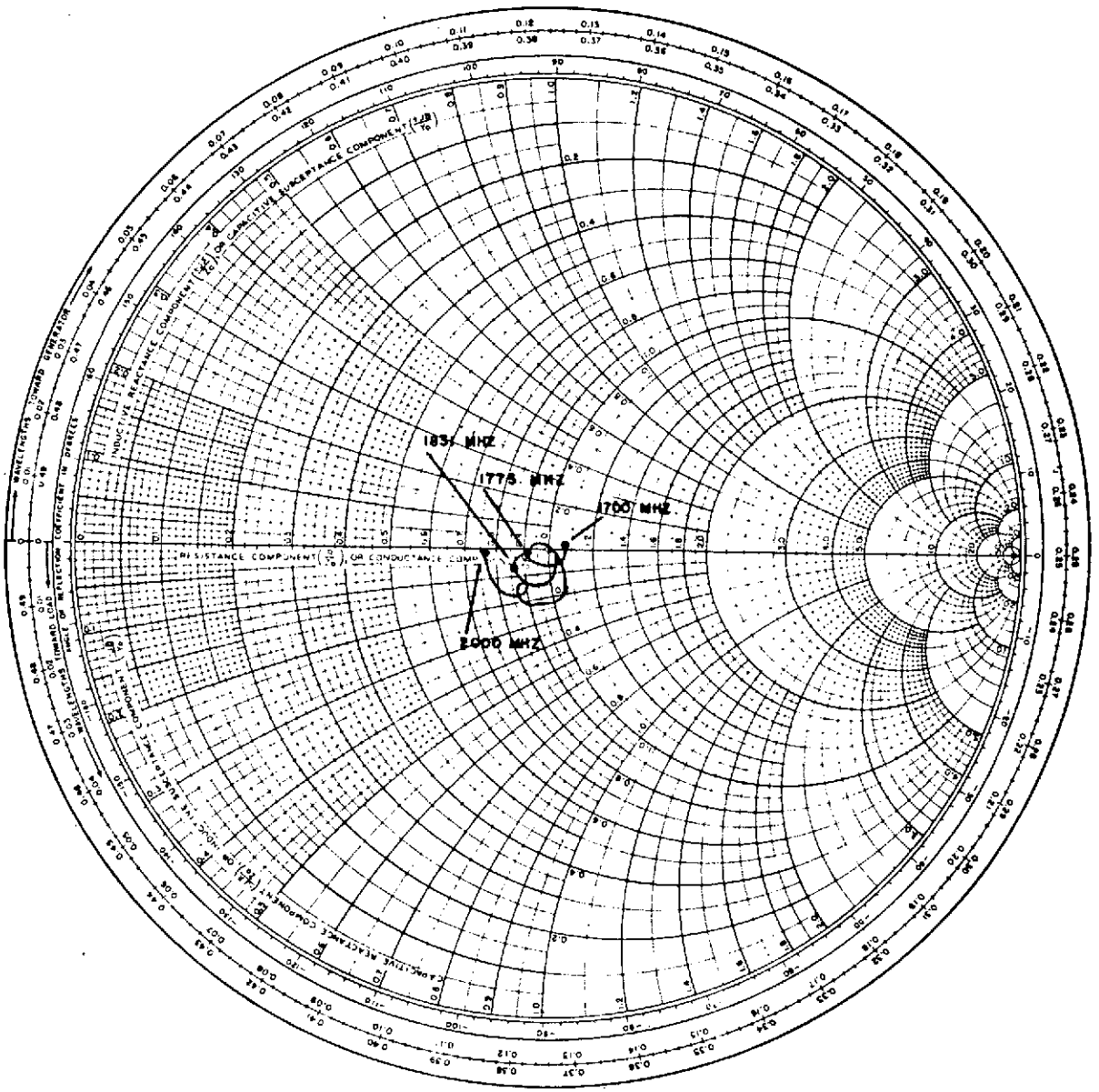

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Figure 4-10. Con't.

B. BREADBOARD ANTENNA

1. Introduction

Three major changes were made to the engineering model to arrive at the breadboard antenna design: (1) the baluns were etched on a single board with inputs accommodating the non-periodic input ports (Figure 4-11); (2) one-half turn of each spiral arm on each spiral was removed to provide increased spacing between the elements for mounting screws (Figure 4-12); and (3) RF manifolds specially made for SPACS I were used. A picture of the breadboard array mounted in the cylindrical ground plane is shown in Figure 4-13.

2. Input Characteristics and Mutual Coupling

Figure 4-14 illustrates the input reflection coefficient as a function of frequency for the central element with all other elements terminated in a load. The VSWR has increased over the engineering model and is as much as 2:1 at certain frequencies. This is primarily due to the design of the balun board. The longer input lines with the several bends contribute the additional mismatch. This can be compared with the results for the engineering model to illustrate a realistic performance level with a better balun design.

Figure 4-15 illustrates the measured mutual coupling between the central element and an adjacent element (elements A7 to A3; refer to Figure 4-16). Note that the coupling has a worst case value of -27.4 dB. This compares with a nominal value of -24 dB for the engineering model. The difference in coupling levels is primarily due to the removal of the half-turns on the spirals.

3. Breadboard Radiation Characteristics

For the purposes of measuring antenna radiation patterns, an outdoor variable length range with a model positioner was used. A picture of this range with the breadboard array being tested is shown in Figure 4-17. A block diagram of the equipment is shown in Figure 4-18. Note that a rotating linear source is used to record circular polarization characteristics.

In order to properly assess the array characteristics with scan, three separate sets of coaxial cables were built: (1) one for broadside, (2) one for 50° (commanded) roll-axis scan, and (3) one for 70° (commanded) nose-to-tail scan. The cable lengths in degreees are shown in Table 4-2. These lengths were determined from the commanded scan angles using a roundoff 3-bit phase shifter quantization algorithm.

Figure 4-19 illustrates the measured array patterns as a function of frequency, plane of cut, and scan angle. Several comments are in order about the obtained pattern results. First note that the 3 dB beamwidth (of the maximum gain envelope) varies between 34° - 38° in the ϕ = 0° cut and 33° - 34.5° in the ϕ = 90° cut. This is compared with nominal theoretical values of 40° (ϕ=0°) and 36° (ϕ= 90°). Secondly, the sidelobes range between -17 and -26 dB from peak at broadside, between -3.5 and -6.5 dB from peak at 50°; and between -6.0 and -8.5 dB from peak at 70°. The high sidelobes in the roll plane are expected theoretically due to the interelement spacing. Thirdly, the axial ratio is quite good having a nominal value of less than 1 dB.

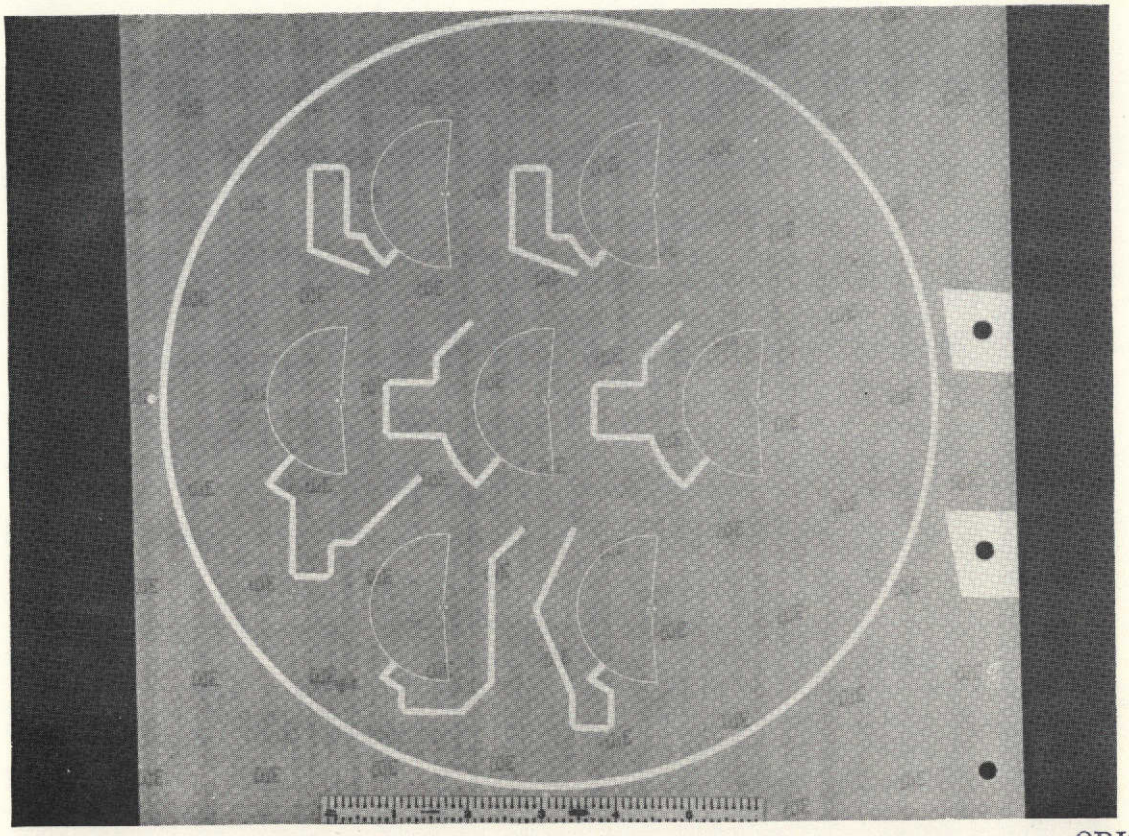

Figure 4-11. Balun Board

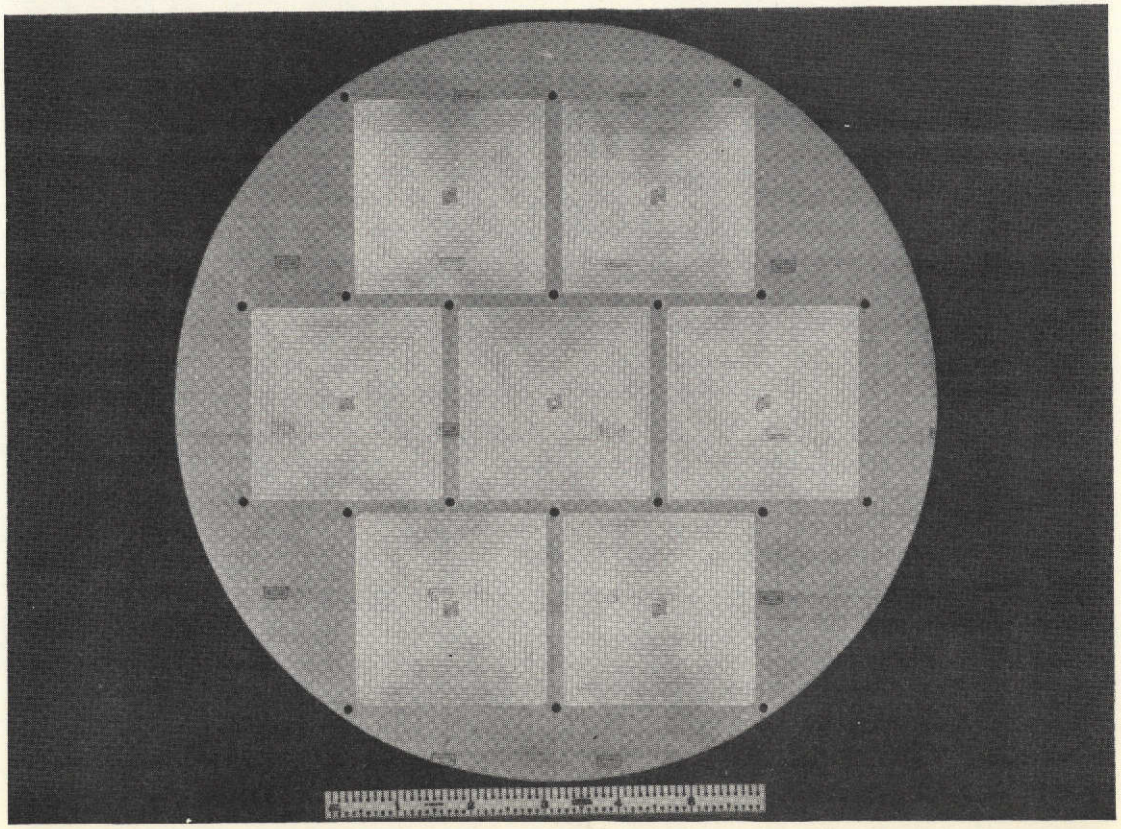

Figure 4-12. Antenna Board

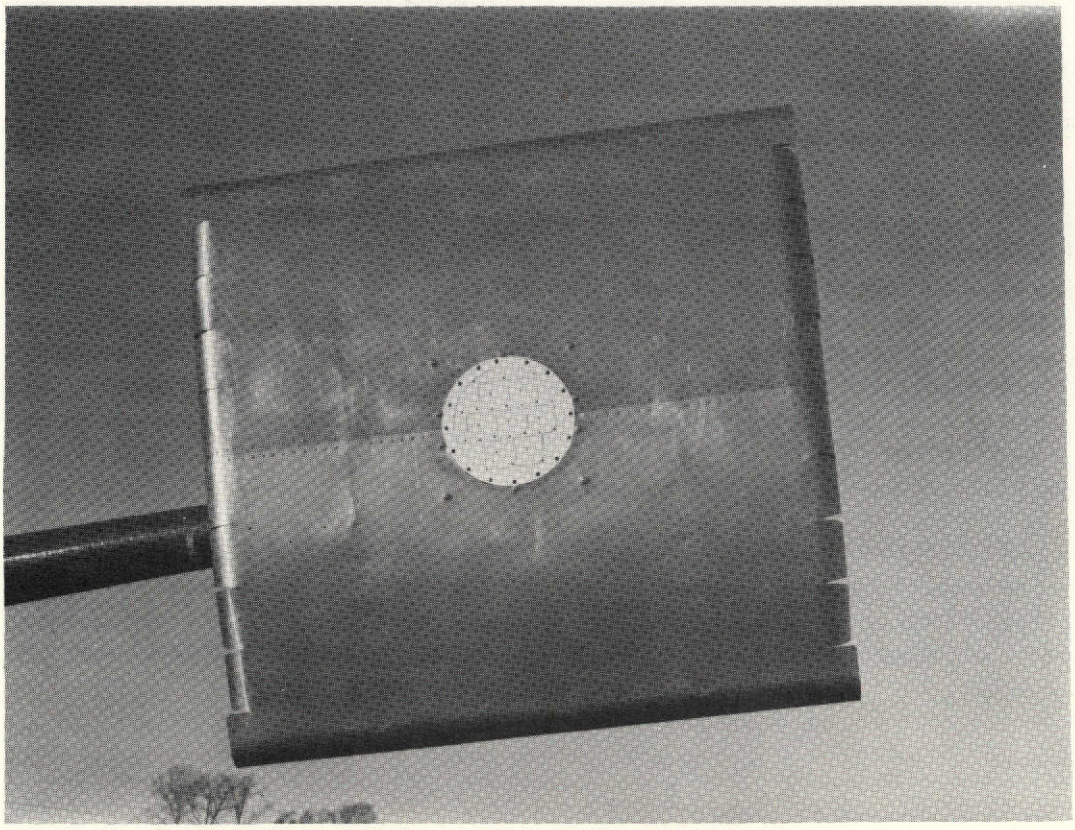

Figure 4-13. SPACS I Antenna in Cylindrical Ground Plane

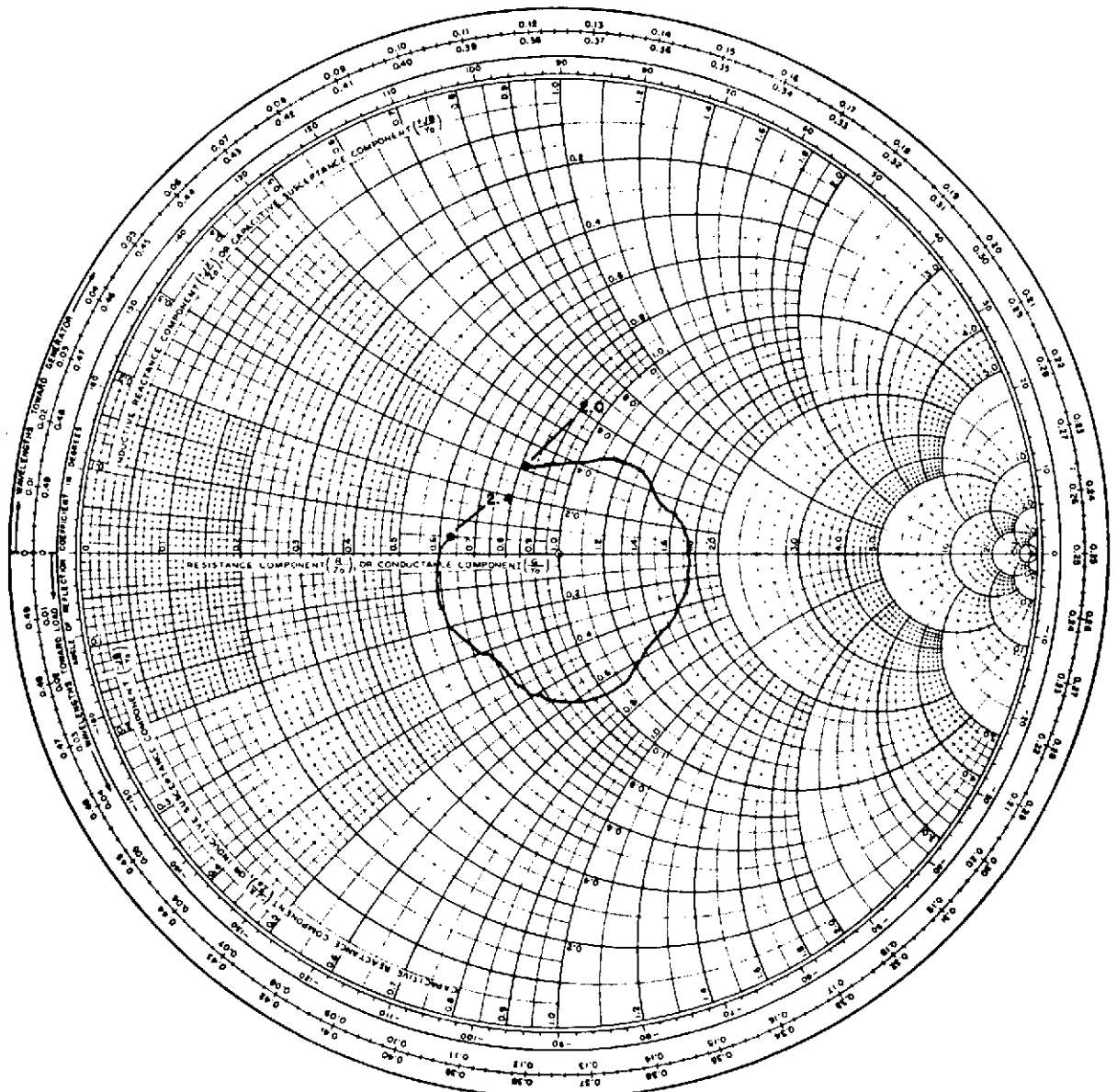

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Figure 4-14. Central Element Impedance for Breadboard Antenna

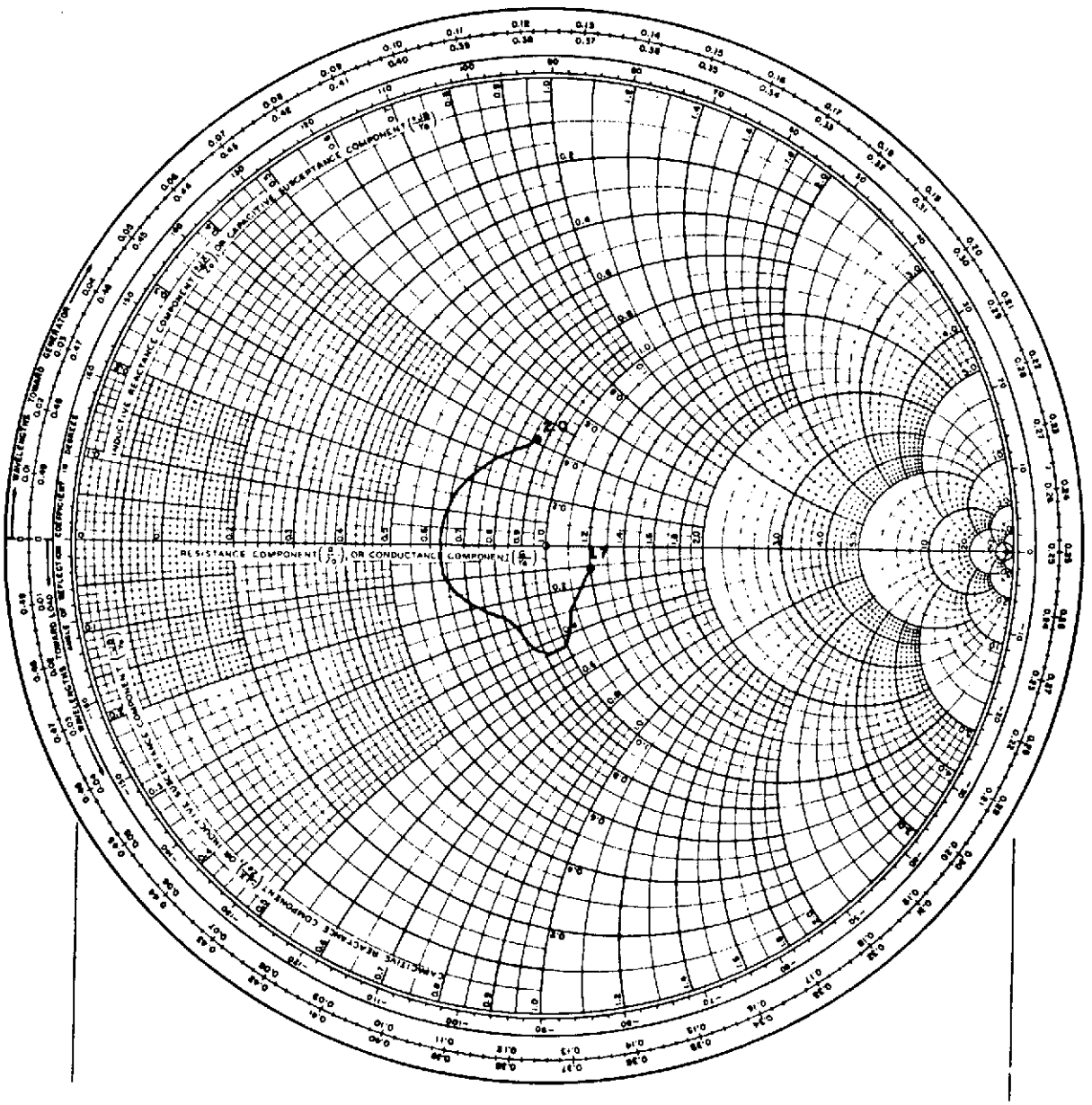

Figure 4-14. Con't.

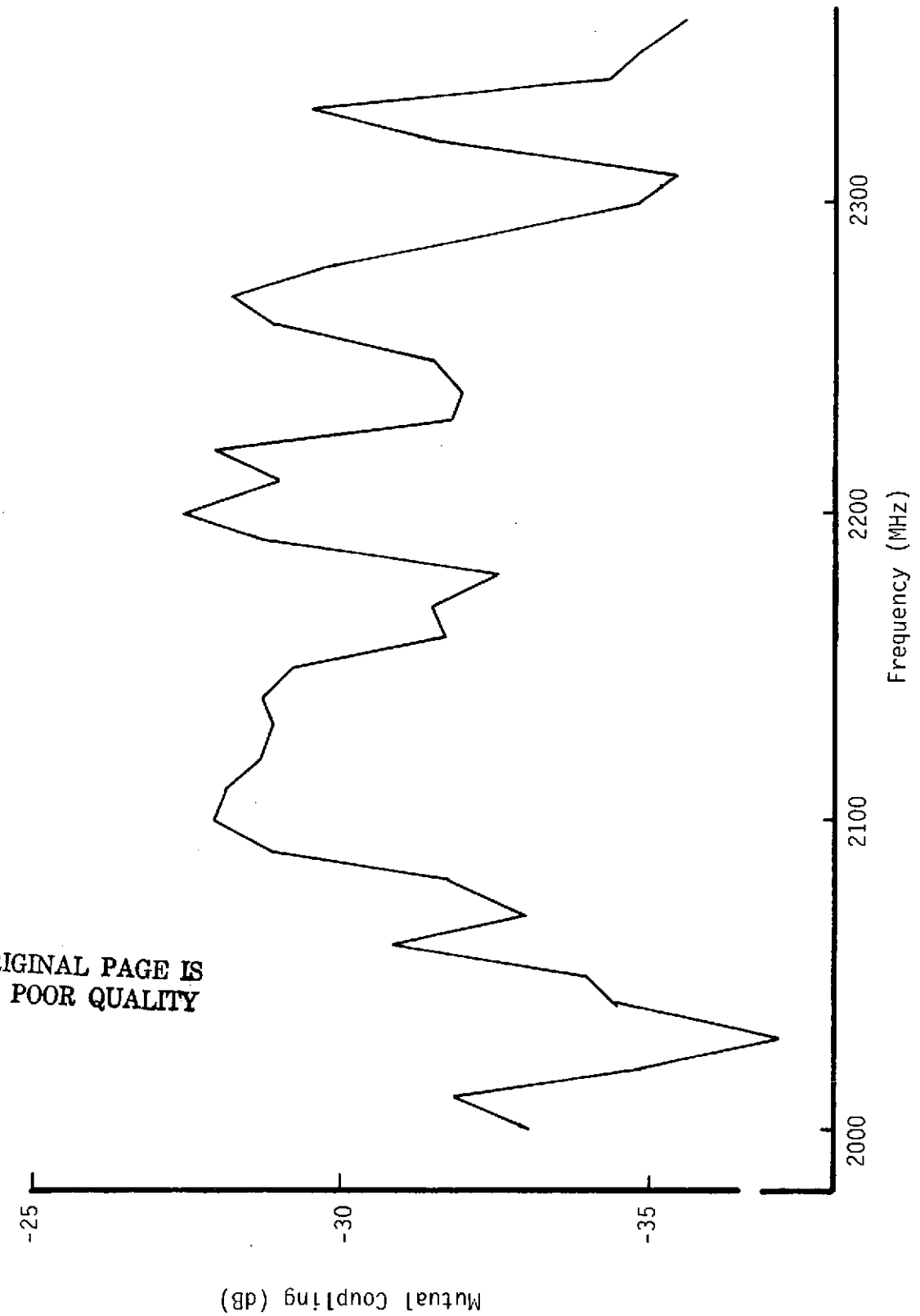

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Figure 4-15. Antenna Mutual Coupling

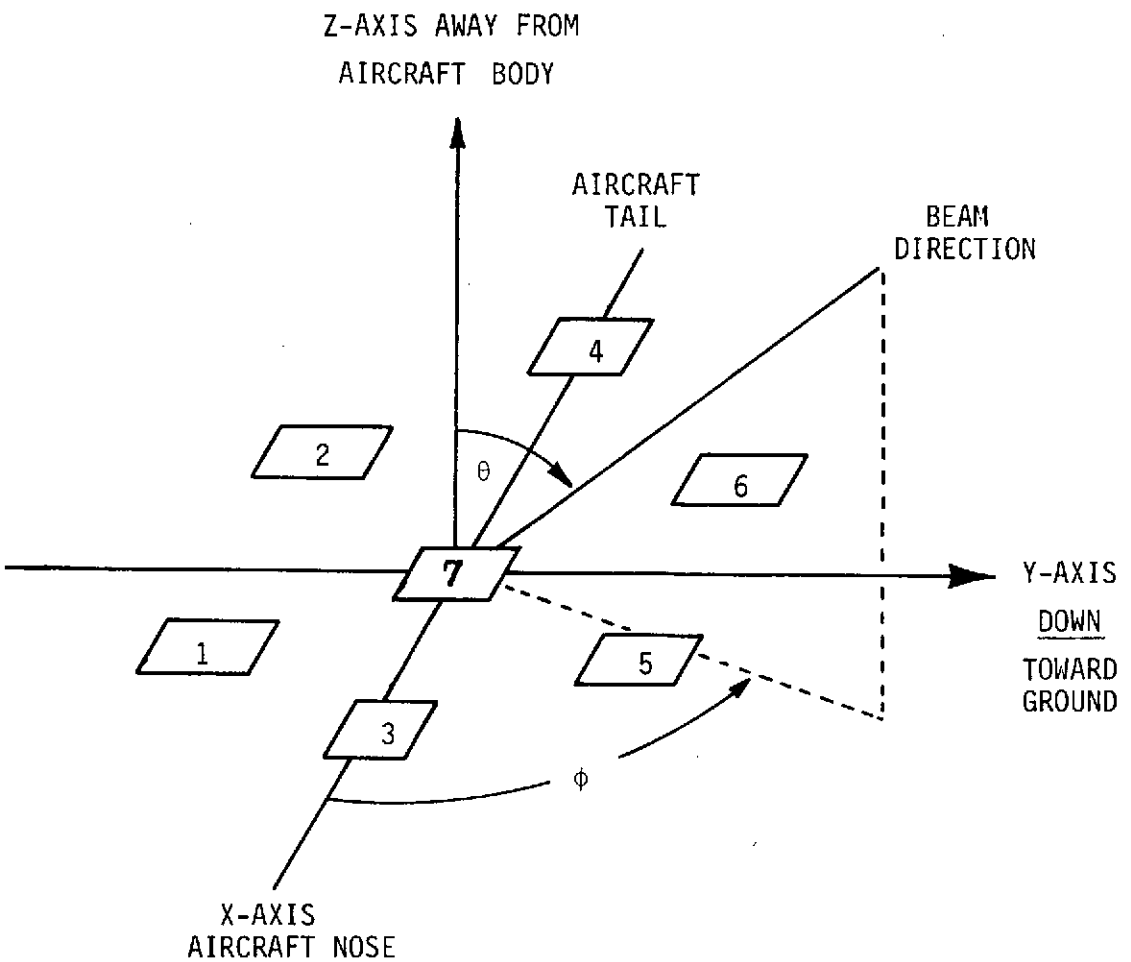

Figure 4-16. Array Steering Geometry

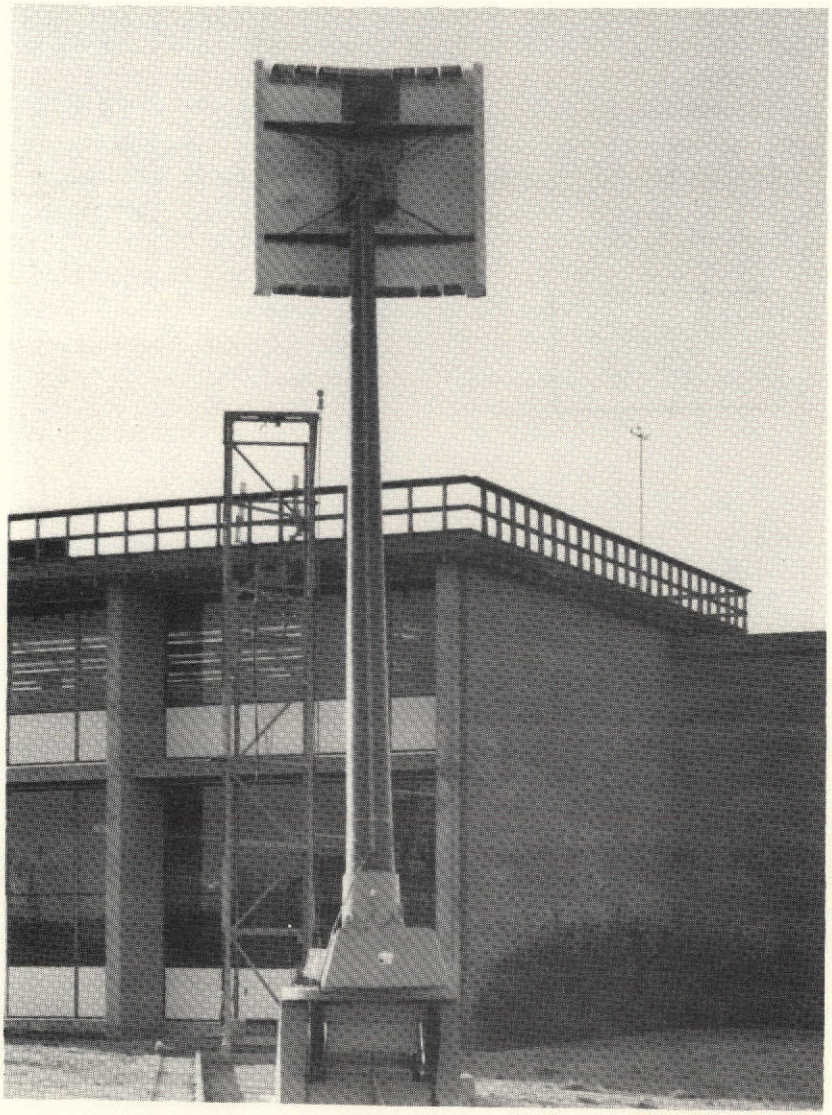

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Figure 4-17. Antenna Range #4

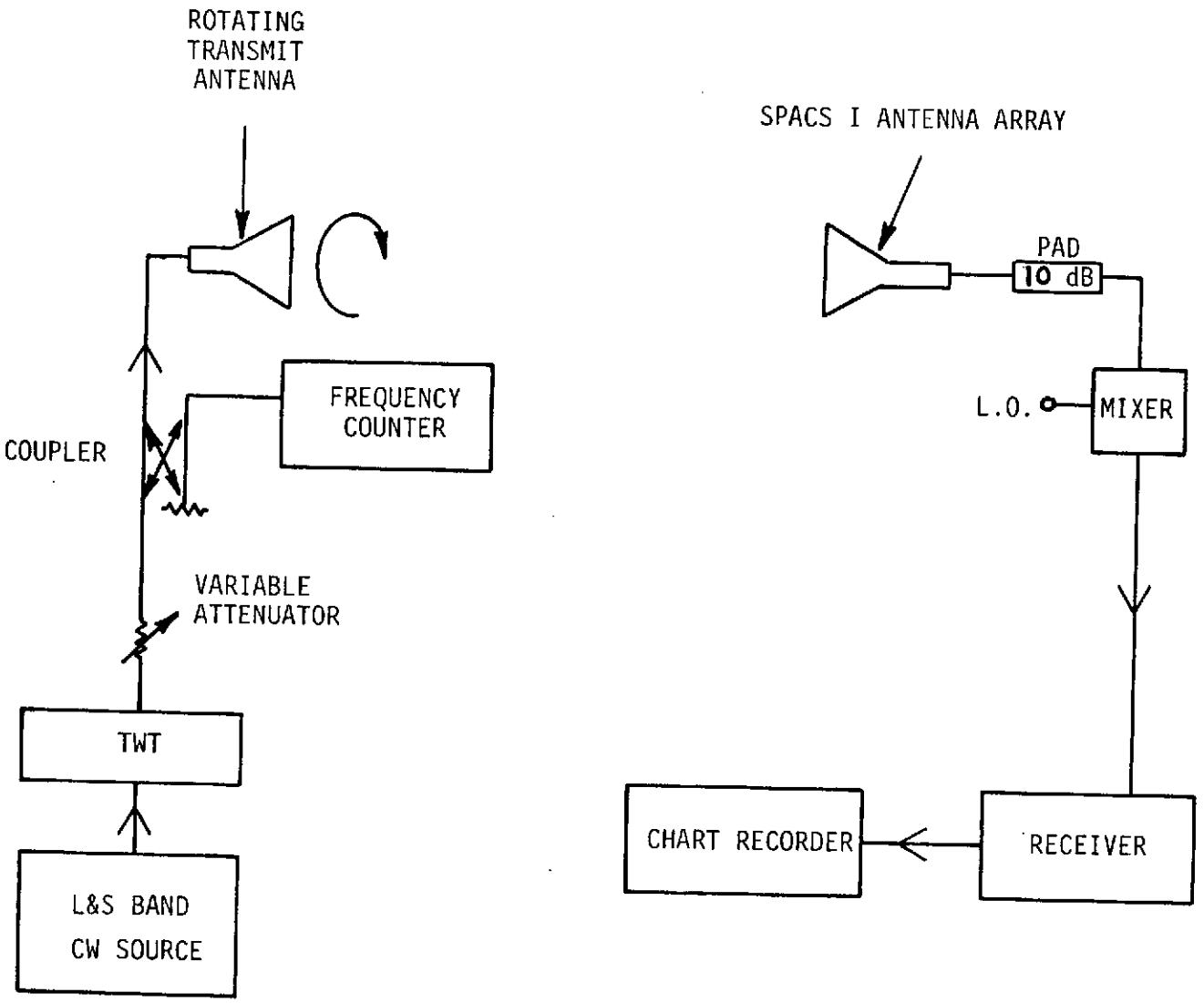

Figure 4-18. Equipment Arrangement for Pattern Tests

Table 4-2. Cable Lengths to Scan Array

ELEMENT	SCAN ANGLE	PHASE
1	50°Roll	135°
2		135°
3		0°
4		0°
5		-135°
6		-135°
7		0°
1	70° Roll	90°
2		-90°
3		180°
4		-180°
5		90°
6		-90°
7		0°

S-Band Transmit Broadside Pattern,
2217.5 MHz, ϕ=90° Cut From Elements
6 and 5 Toward Elements 1 and 2.

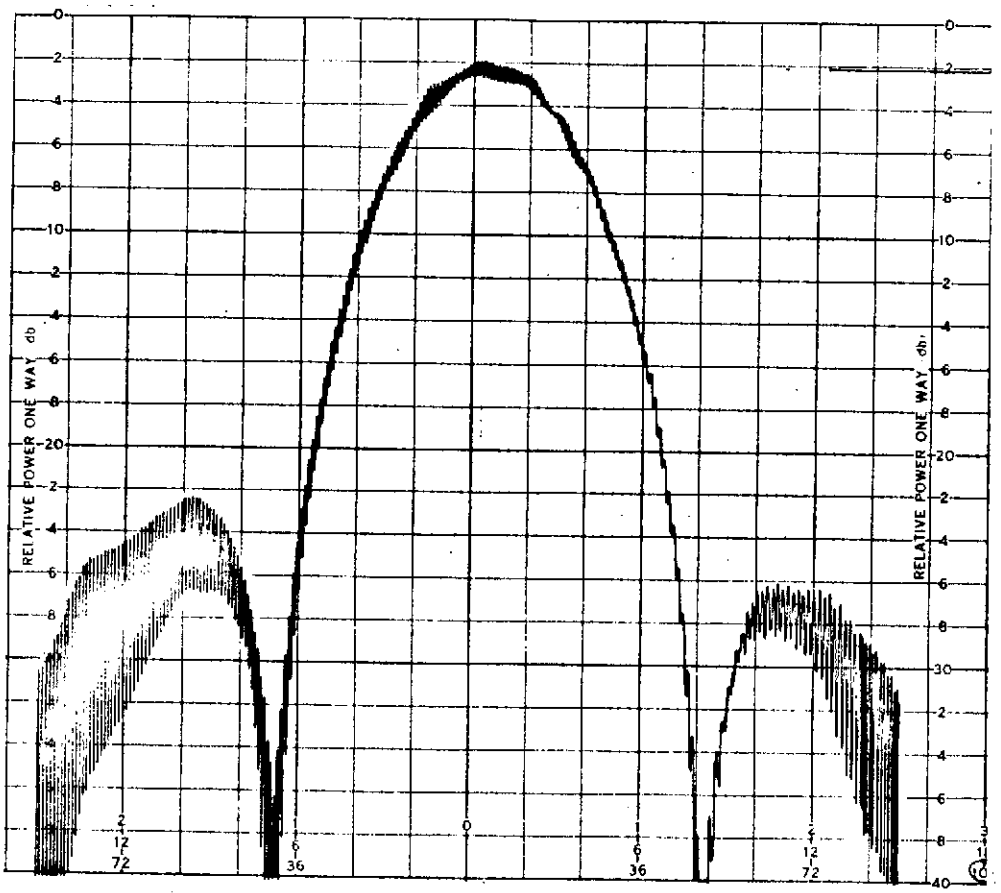

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Figure 4-19. SPACS I Seven Element Array S-Band Patterns
(Transmit and Receive)

S-Band Transmit Broadside Pattern,
2217.5 MHz, ϕ=0° Cut From Element
4 Toward Element 3.

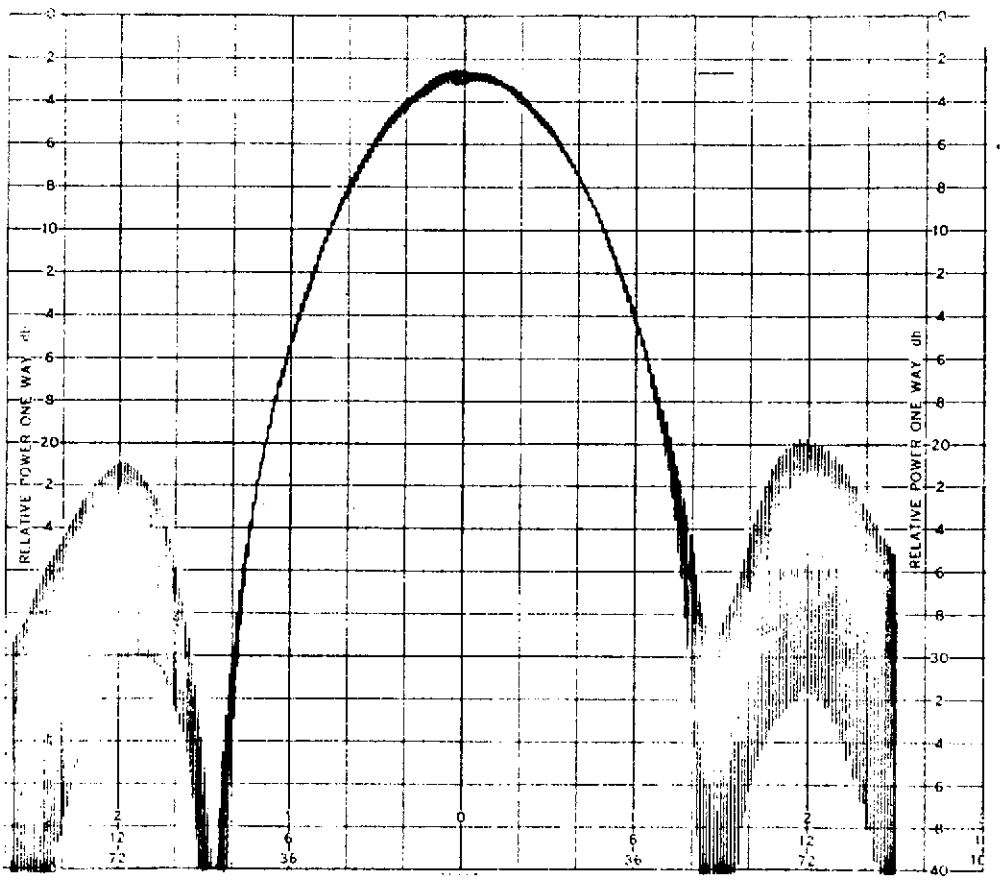

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Figure 4-19. Continued

S-Band Transmit Broadside Pattern,
2287.5 MHz, ϕ=0° Cut From Element
4 Toward Element 3.

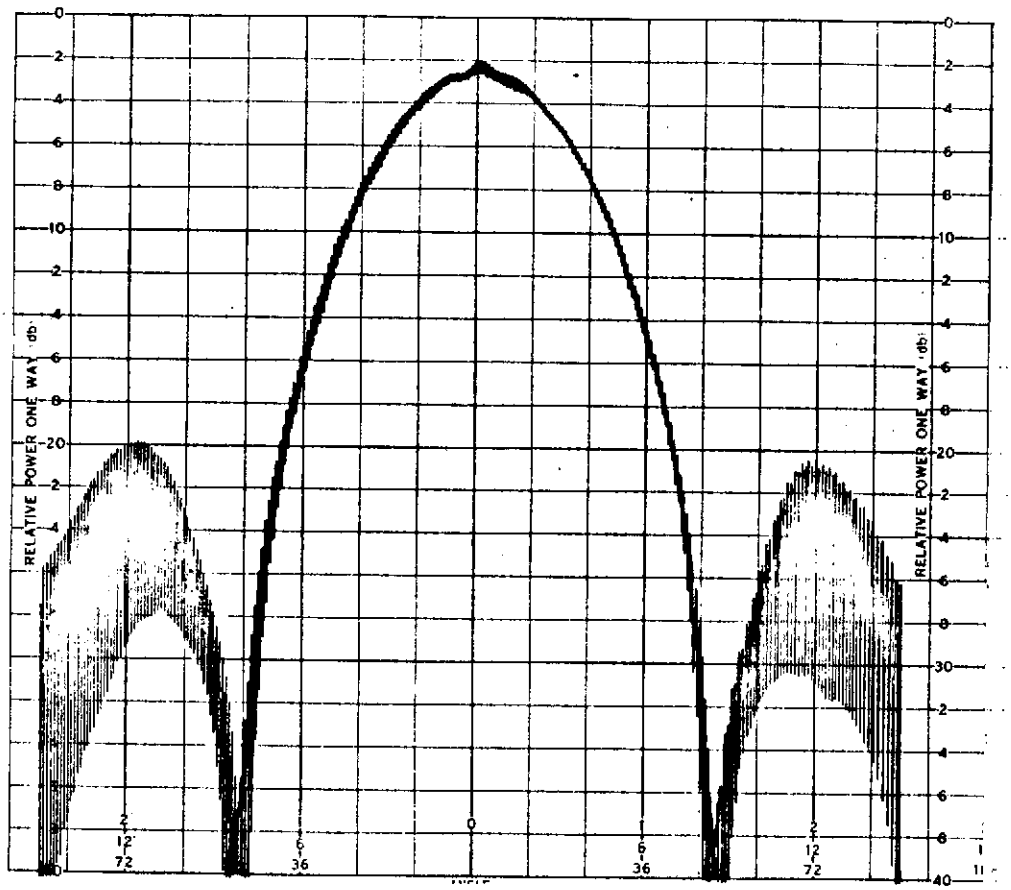

Figure 4-19. Continued

S-Band Transmit Broadside Pattern,
2287.5 MHz, ϕ=90° Cut From Elements
6 and 5 Toward Elements 1 and 2.

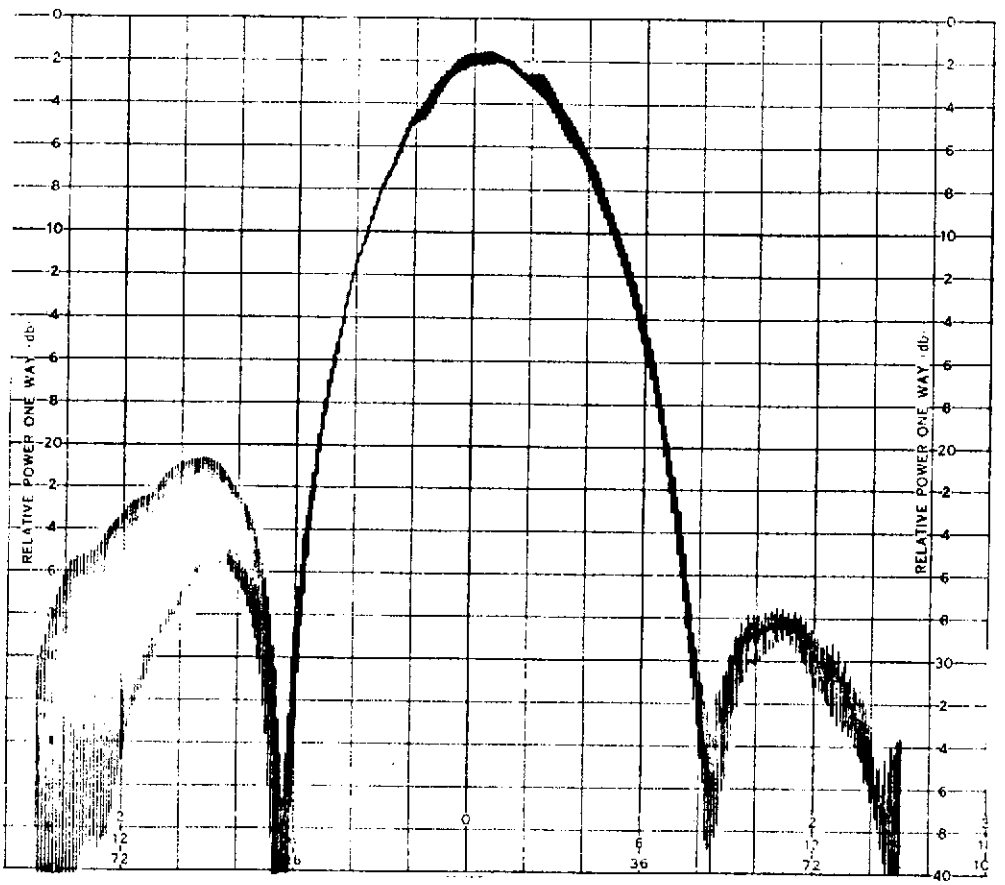

Figure 4-19. Continued

S-Band Receive Broadside Pattern,
2041.9 MHz, ϕ=90° Cut From Elements
6 and 5 Toward Elements 1 and 2.

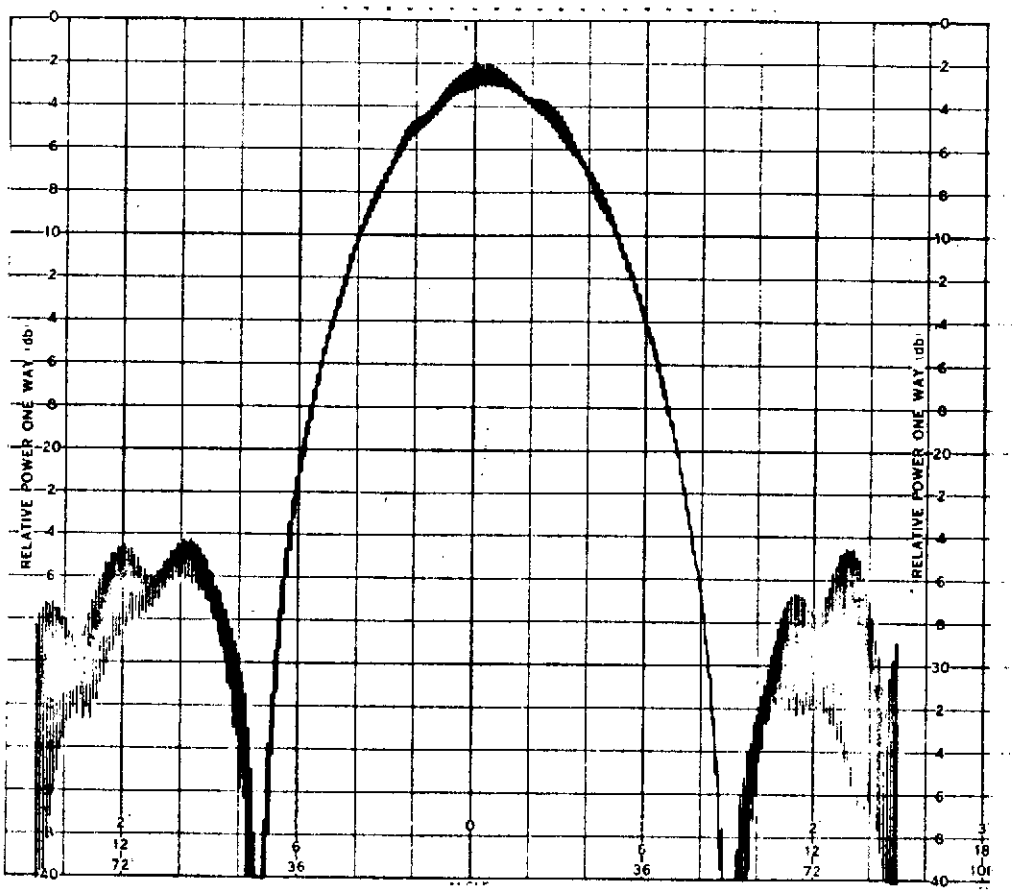

Figure 4-19. Continued

S-Band Receive Broadside Pattern,
2041.9 MHz, ϕ=0° Cut From Element
4 Toward Element 3.

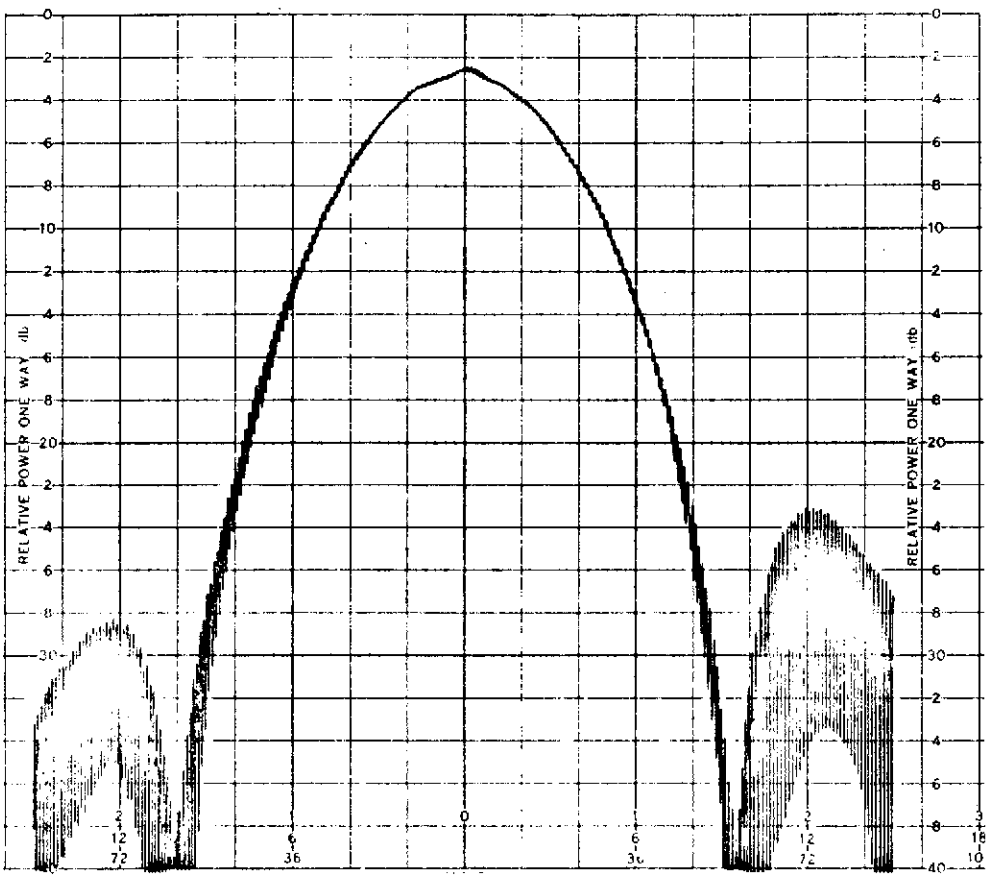

Figure 4-19. Continued

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S-Band Receive Broadside Pattern,
2106.4 MHz, ϕ=0° Cut From Element
4 Toward Element 3.

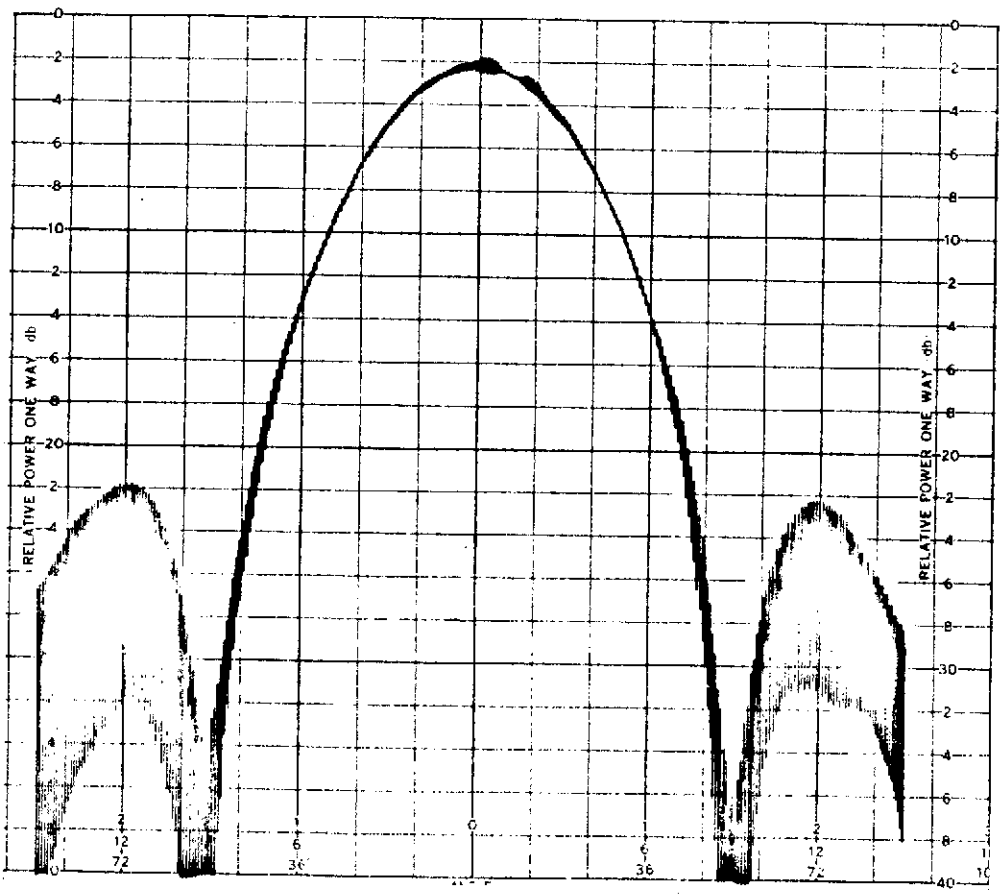

Figure 4-19. Continued

S-Band Receive Broadside Pattern,
2106.4 MHz, ϕ=90° Cut From Elements
5 and 6 Toward 1 and 2.

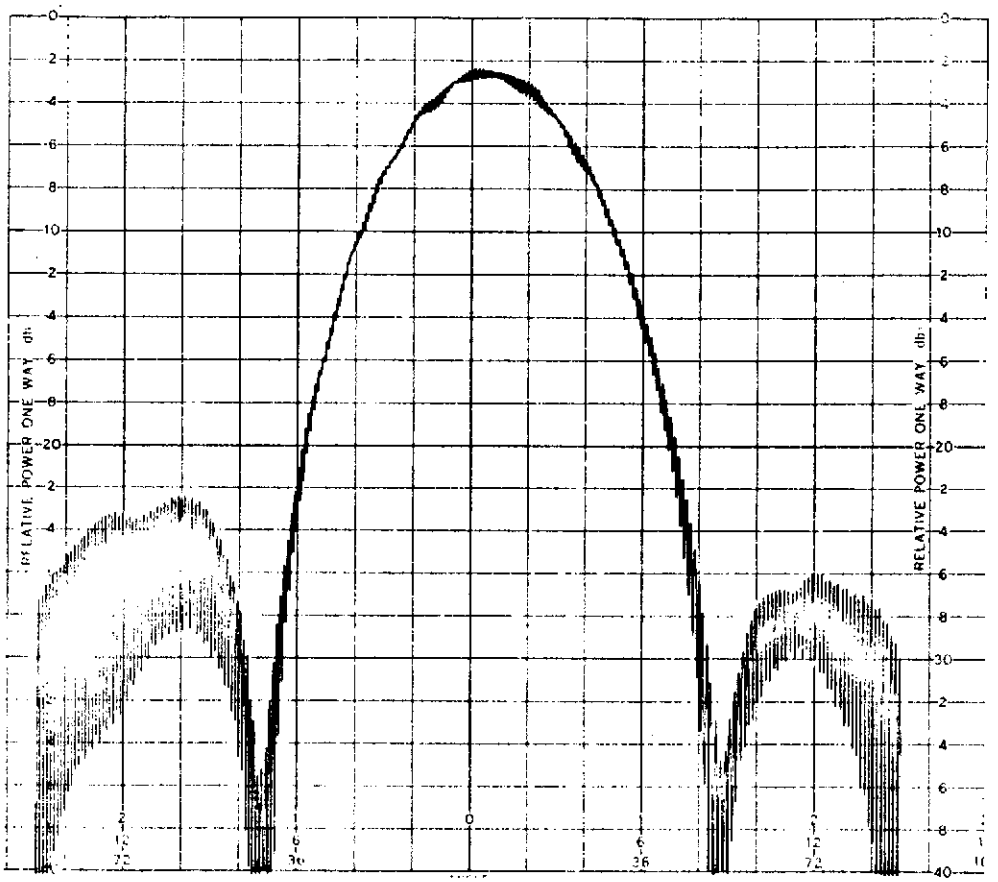

Figure 4-19. Continued

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S-Band Transmit 50° Scan Pattern,
2217.5 MHz, ϕ=90° Cut From Elements
5 and 6 Toward Elements 1 and 2.

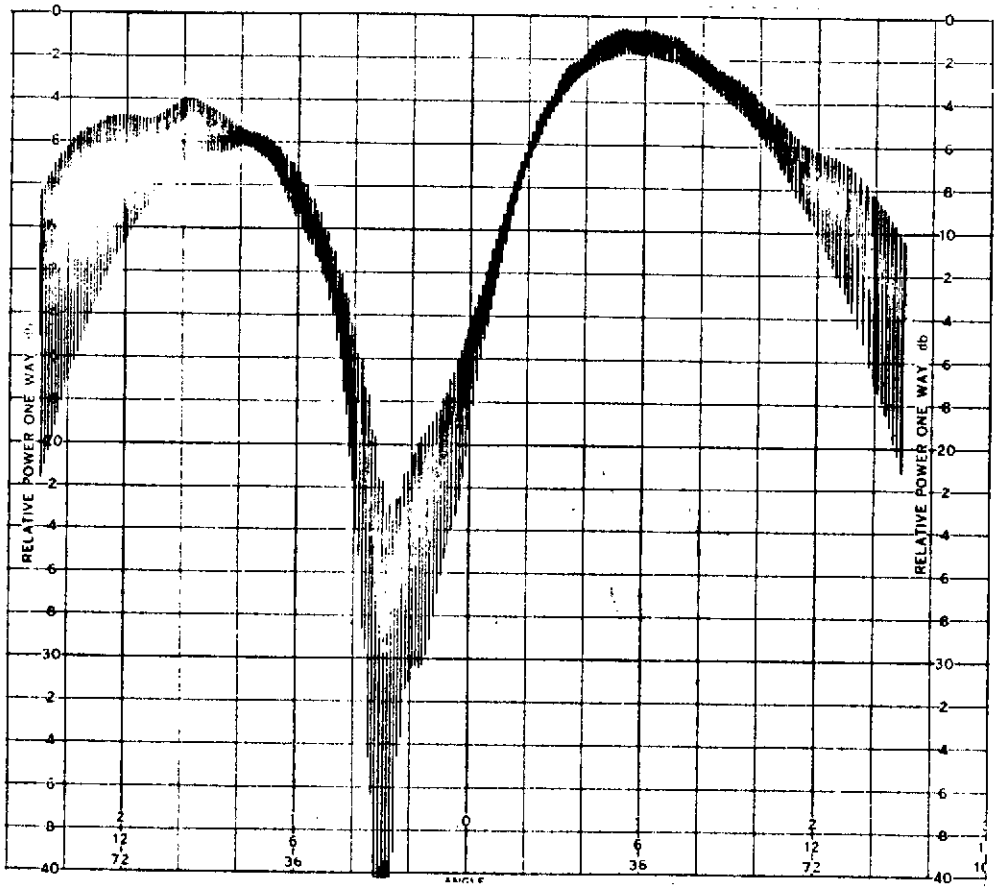

Figure 4-19. Continued

S-Band Transmit 50° Scan Pattern,
2287.5 MHz, ϕ=90° Cut From Elements
5 and 6 Toward Elements 1 and 2.

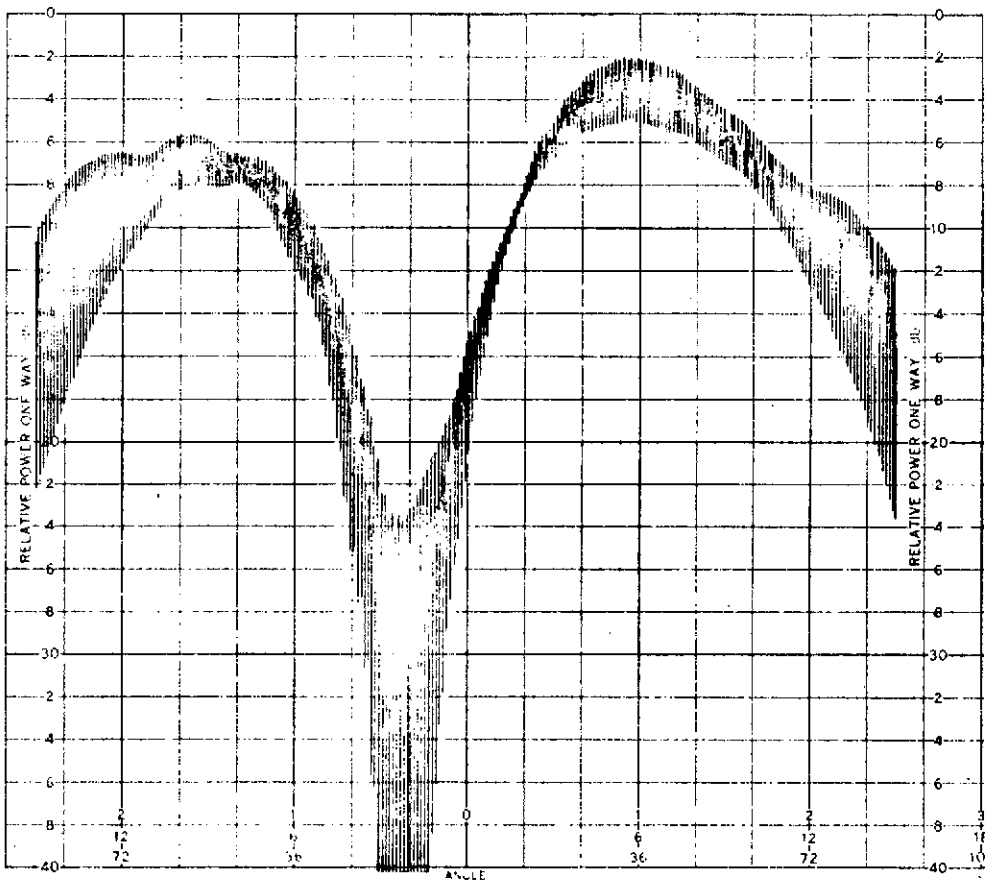

Figure 4-19. Continued

S-Band Receive 50° Scan Pattern,
2041.9 MHz, ϕ=90° Cut From Elements
5 and 6 Towards Elements 1 and 2.

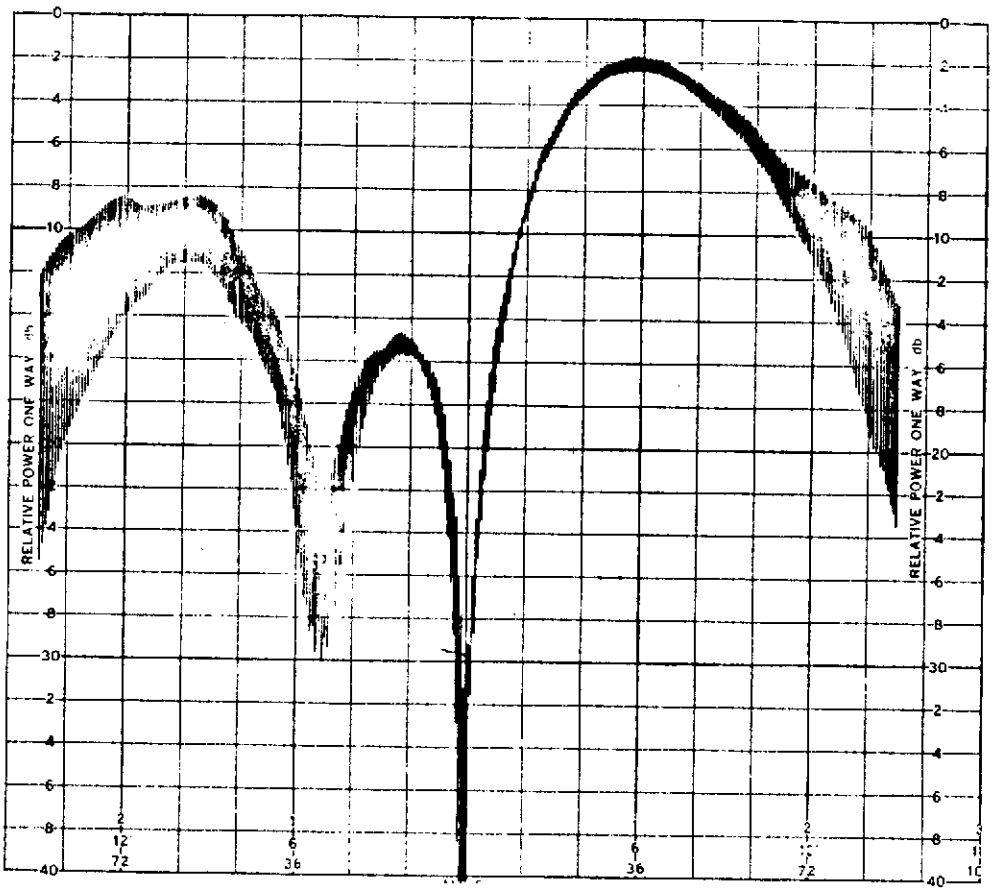

Figure 4-19. Continued

S-Band Receive 50° Scan Pattern,
2106.4 MHz, ϕ=90° Cut From Elements
5 and 6 Toward Elements 1 and 2.

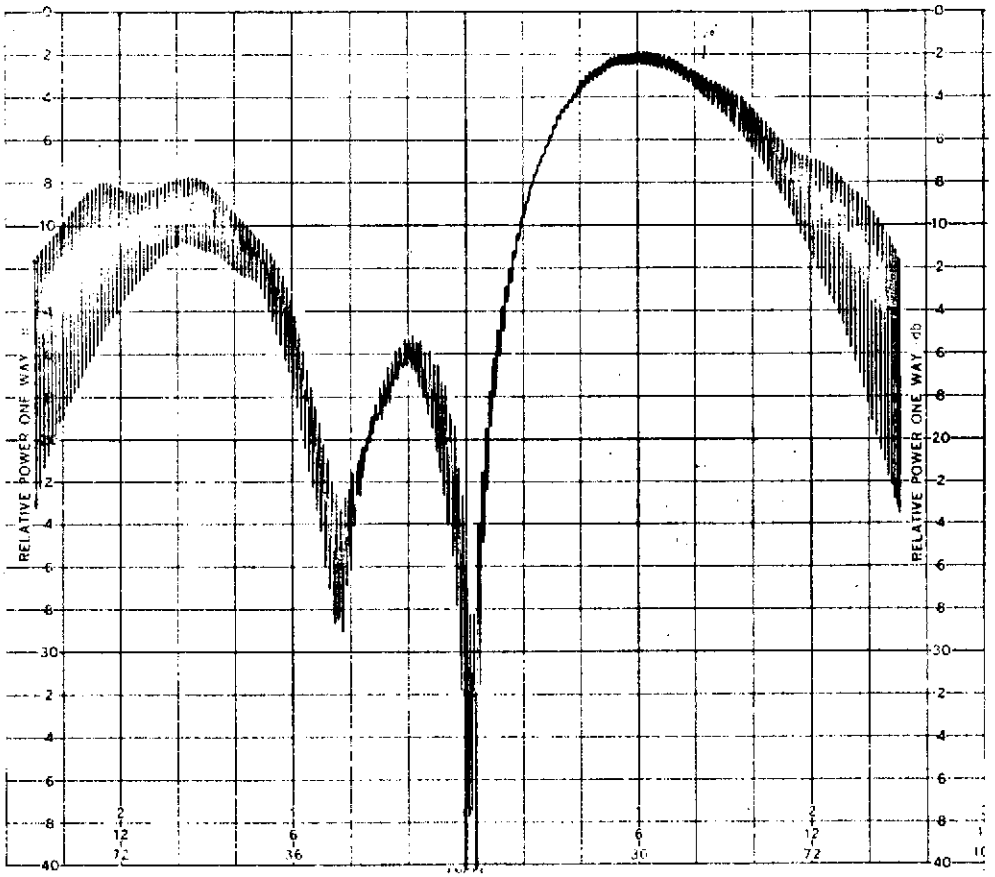

Figure 4-19. Continued

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S-Band Receive 70° Scan Pattern,
2041.9 MHz, ϕ=0° Cut From Element
4 Toward Element 3.

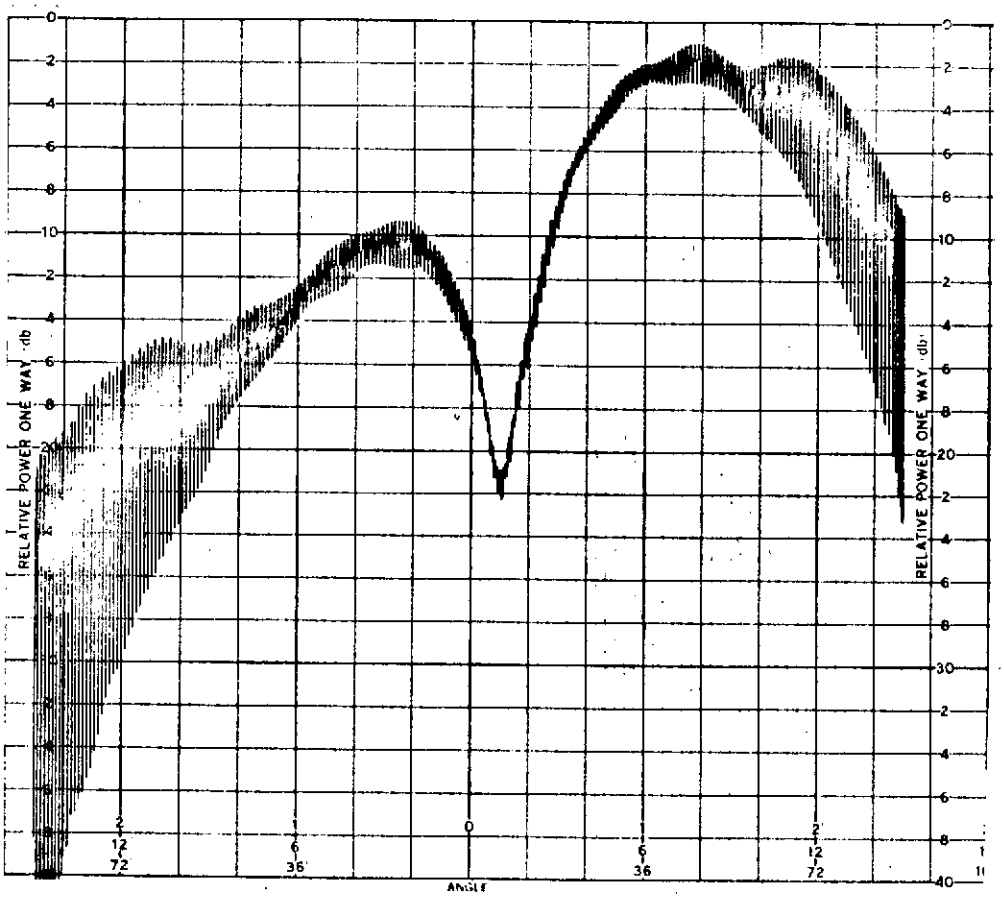

Figure 4-19. Continued

S-Band Receive 70° Scan Pattern,
2106.4 MHz, ϕ=0° Cut From Element
4 Toward Element 3.

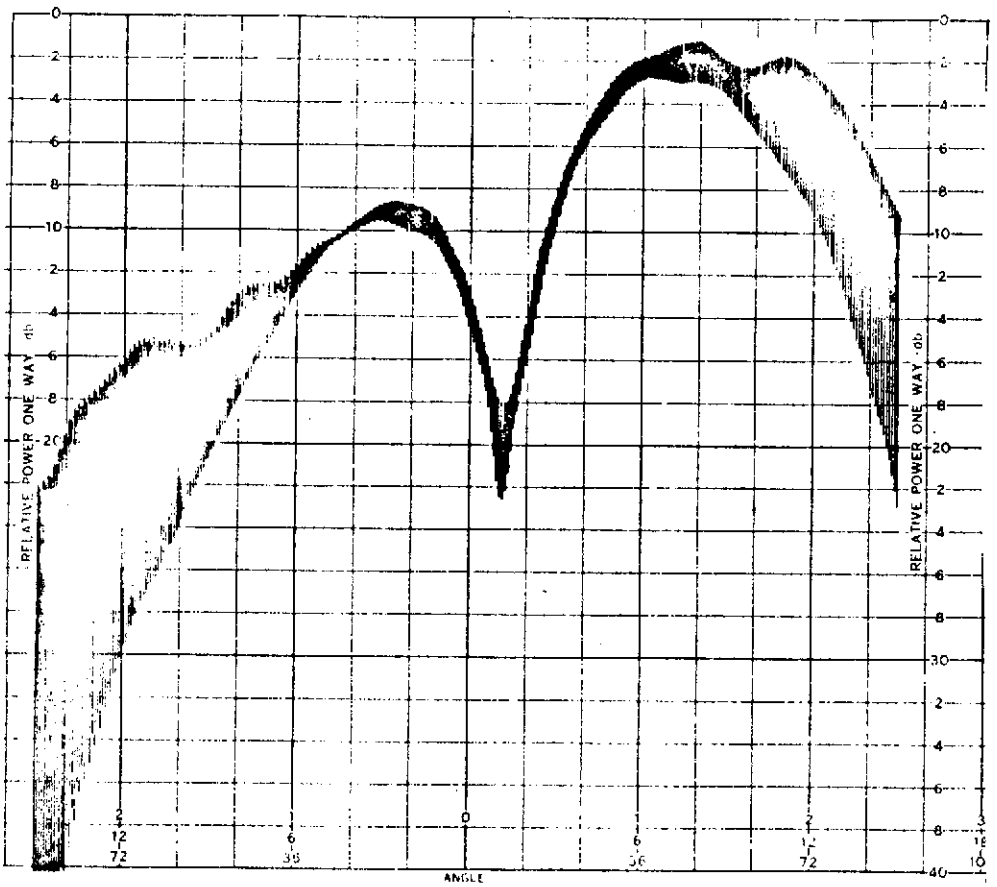

Figure 4-19. Continued

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S-Band Transmit 70° Scan Pattern,
2217.5 MHz, ϕ=0° Cut From Element
4 Toward 3.

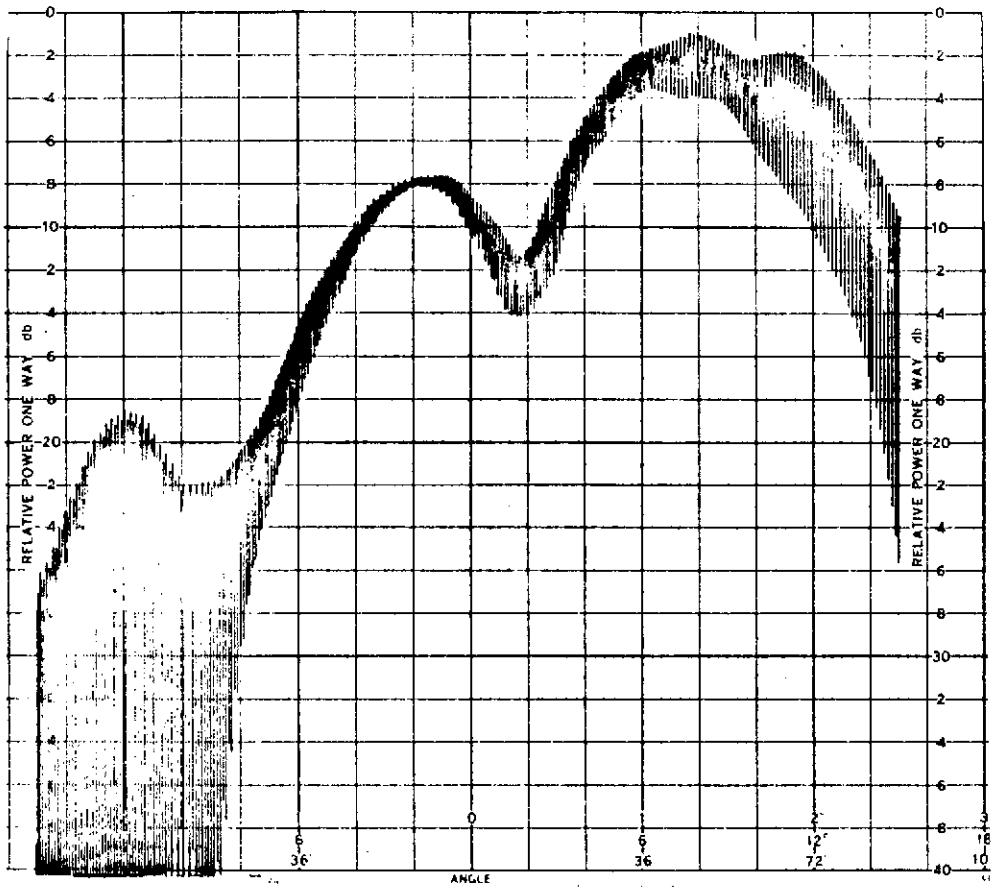

Figure 4-19. Continued

S-Band Transmit 70° Scan Pattern,
2287.5 MHz, ϕ=0° Cut From Element
4 Toward Element 3.

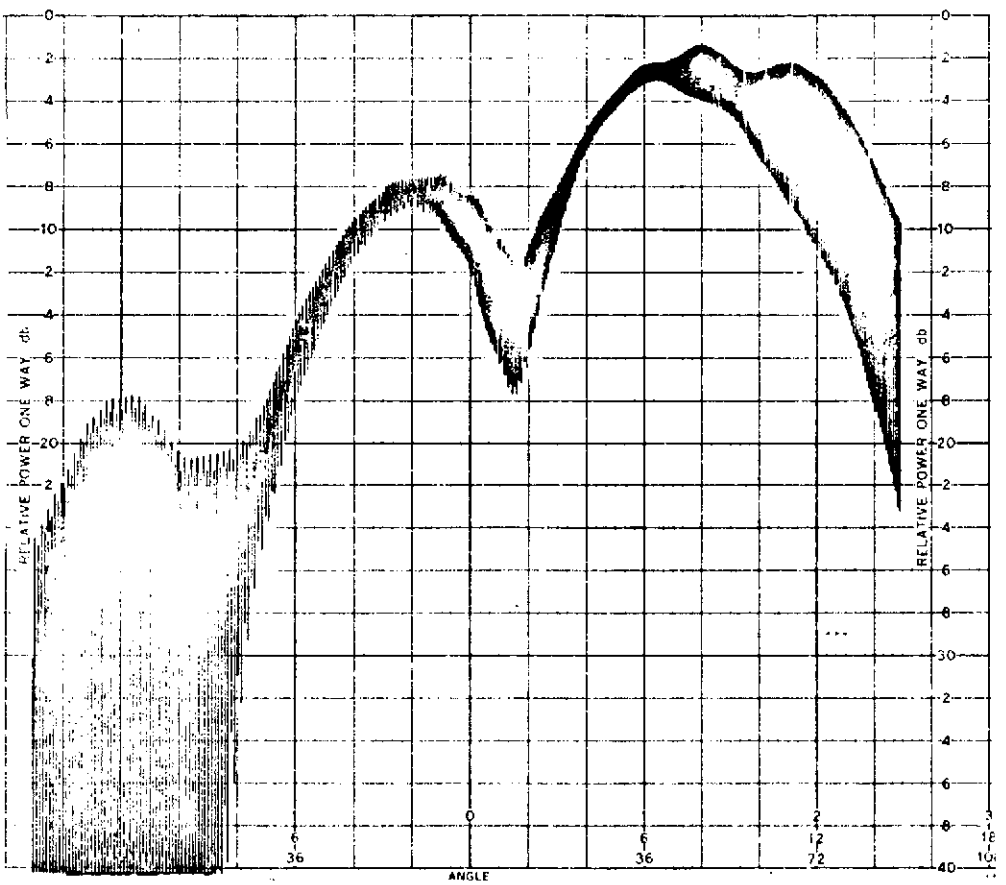

Figure 4-19. Continued

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The central element patterns for L-band operation are shown in Figure 4-20. The element patterns have dips in gain at boresight. This is a typical low-frequency mutual coupling effect. The isolated element pattern at these frequencies has a cosθ shape. Figure 4-21 illustrates the central element pattern at the S-band frequencies. At the higher frequencies, the patterns become flatter and more like an isolated element pattern.

4. Breadboard Gain and Axial Ratio

For gain measurements, a slightly different experimental setup is used as shown in Figure 4-22. This setup uses an RF switch to allow comparison of the array data with a standard gain horn. Figure 4-23 is a picture of the back of the array showing the standard gain horn mounted on the back of the array.

The matched circularly polarized gain is defined to be:

$$G_{cp} = G_{linear} + B + M + C$$

where

$G_{linear} = G_{SCH} - \Delta_{dB}$

G_{SCH} = linear gain of standard gain horn

Δ_{dB} = difference between maximum gain envelope and standard gain horn

and

$B = 10 \log(1+r^2)$

$r = 10^{-a/20}$

a = axial ratio in dB

and

M = manifold loss in dB

C = cable loss in dB.

Figure 4-24 shows the array gain over the frequency band of interest for broadside scan. When compared with the engineering model results (Figure 4-8), the gain is generally about 1 dB lower. This is due primarily to : (1) the increased reflections in the balun board, (2) the longer lines of the balun board (creating more loss), and (3) the protective paint on the spirals is lossy. In addition to this loss in gain, the gain no longer monotonically increases. Indeed, the gain is maximum at about 2160 MHz. This is the center frequency of the balun. This and other evidence points to the fact that this phenomena is due to the balun board design and not the spiral array.

Figure 4-25 illustrates the array axial ratio vs. frequency for the broadside scan. It is generally under 1 dB which is an improvement over the engineering model. This is due in part to the loading provided by paint. It is also due to the better construction of the breadboard array.

Central Element Pattern, 1775.5 MHz,
ϕ=0° Cut From Element 4 Toward
Element 3.

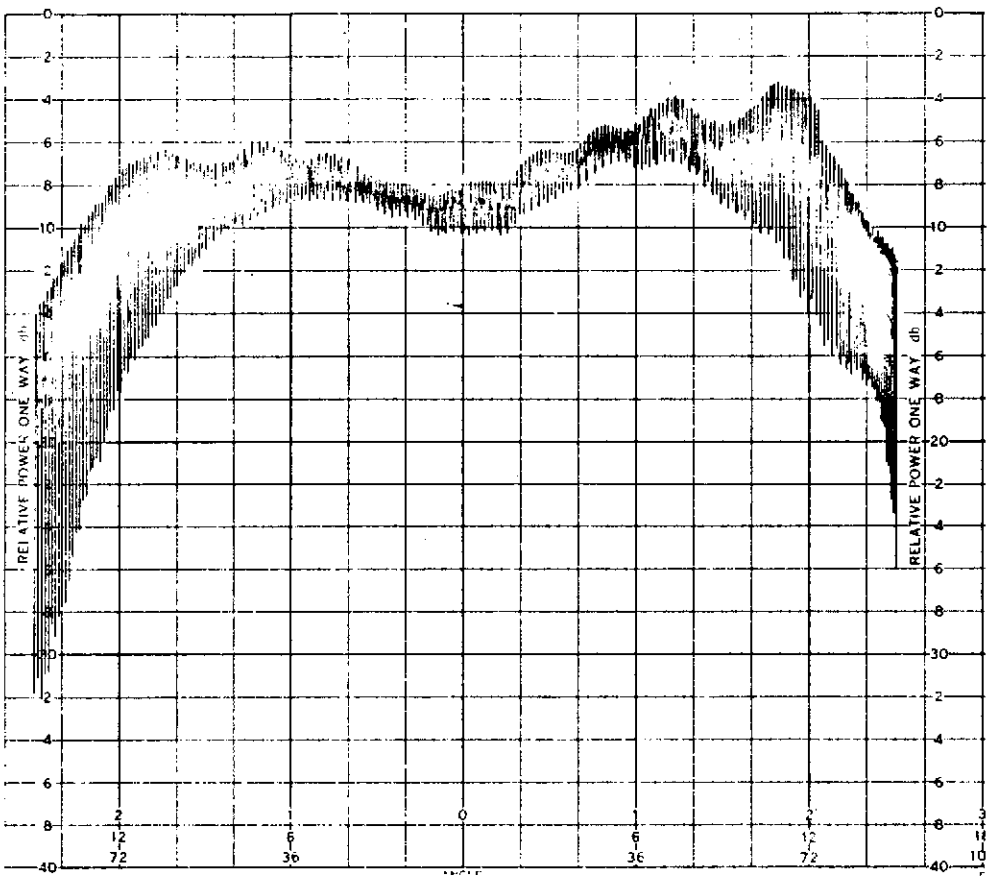


Figure 4-20. SPACS I Central Element L-Band Patterns In Array

Central Element Pattern, 1775.5 MHz,
ϕ=90° Cut From Elements 5 and 6
Toward Elements 1 and 2.

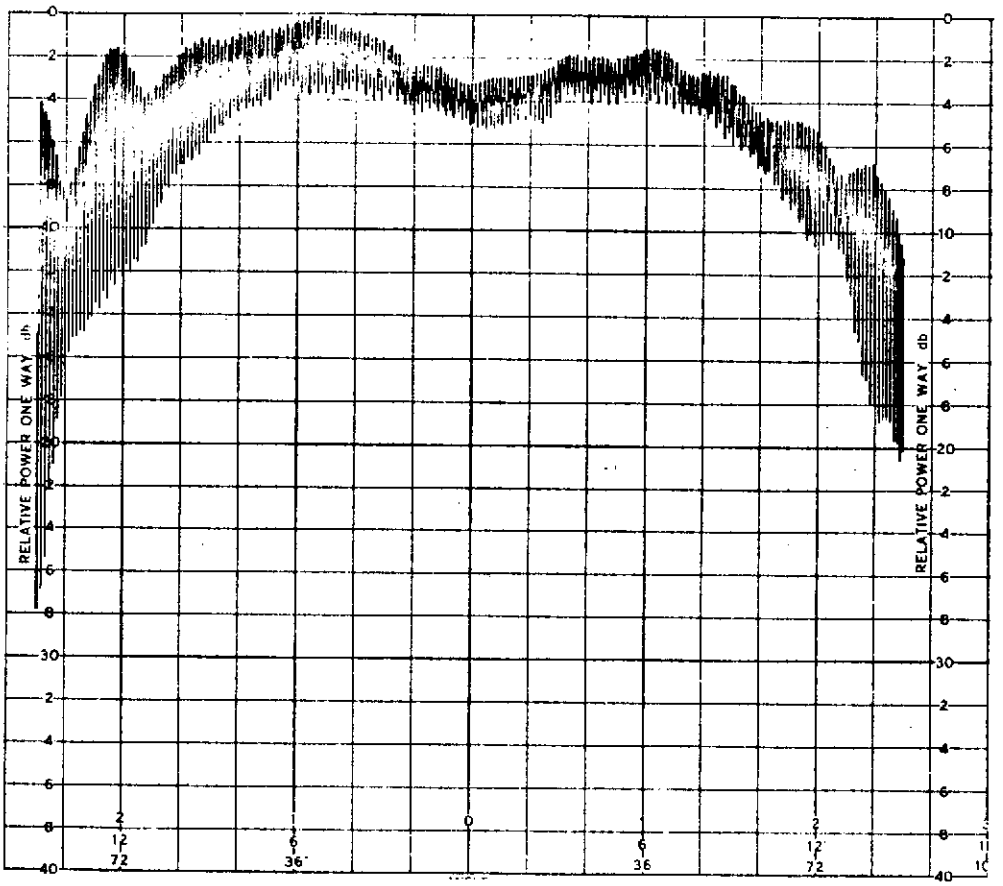


Figure 4-20. Continued

Central Element Pattern, 1831.8 MHz,
ϕ=0° Cut From Element 4 Toward
Element 3.

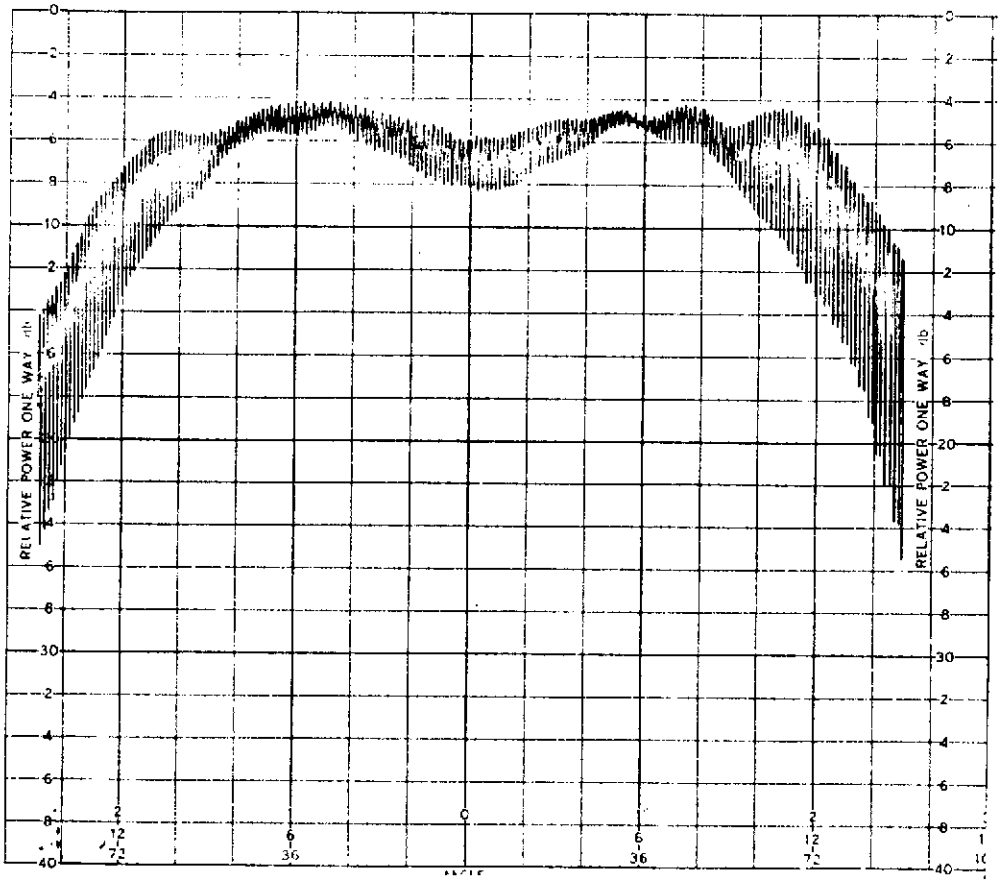


Figure 4-20. Continued

Central Element Pattern, 1831.8 MHz,
ϕ=90° Cut From Elements 5 and 6
Toward Elements 1 and 2.

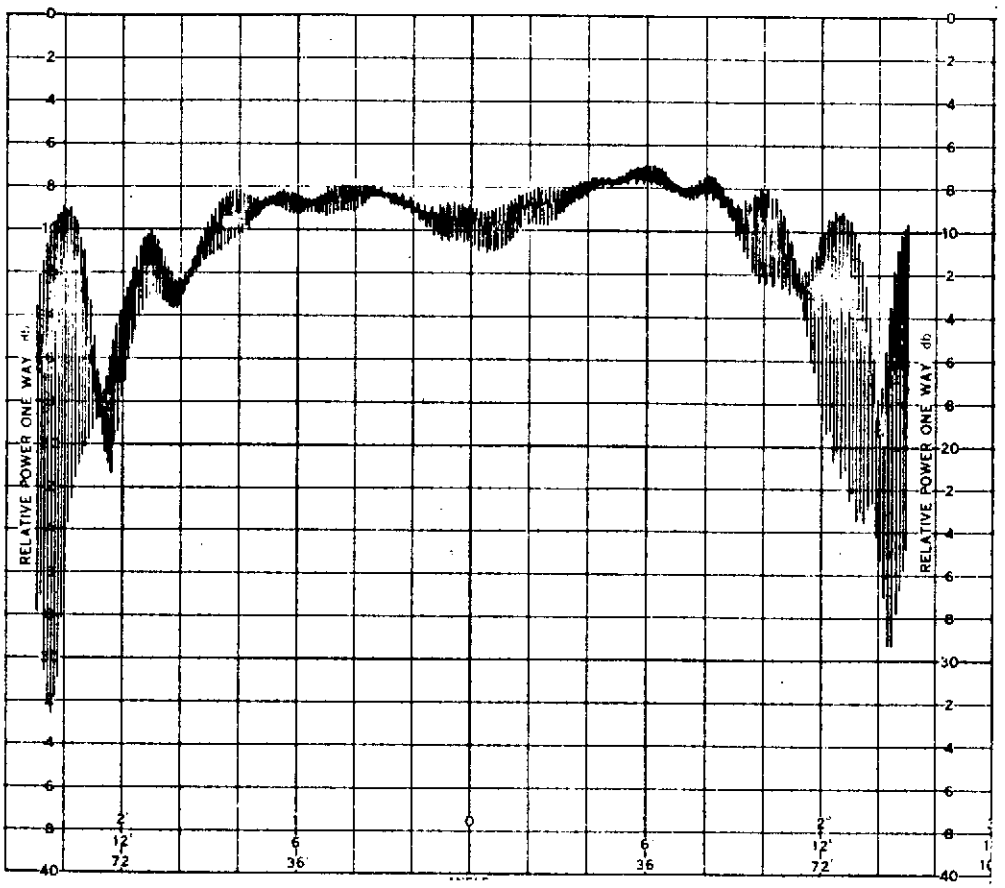


Figure 4-20. Continued

Central Element Pattern, 2041.9 MHz,
ϕ=0° Cut From Element 4 Toward
Element 3.

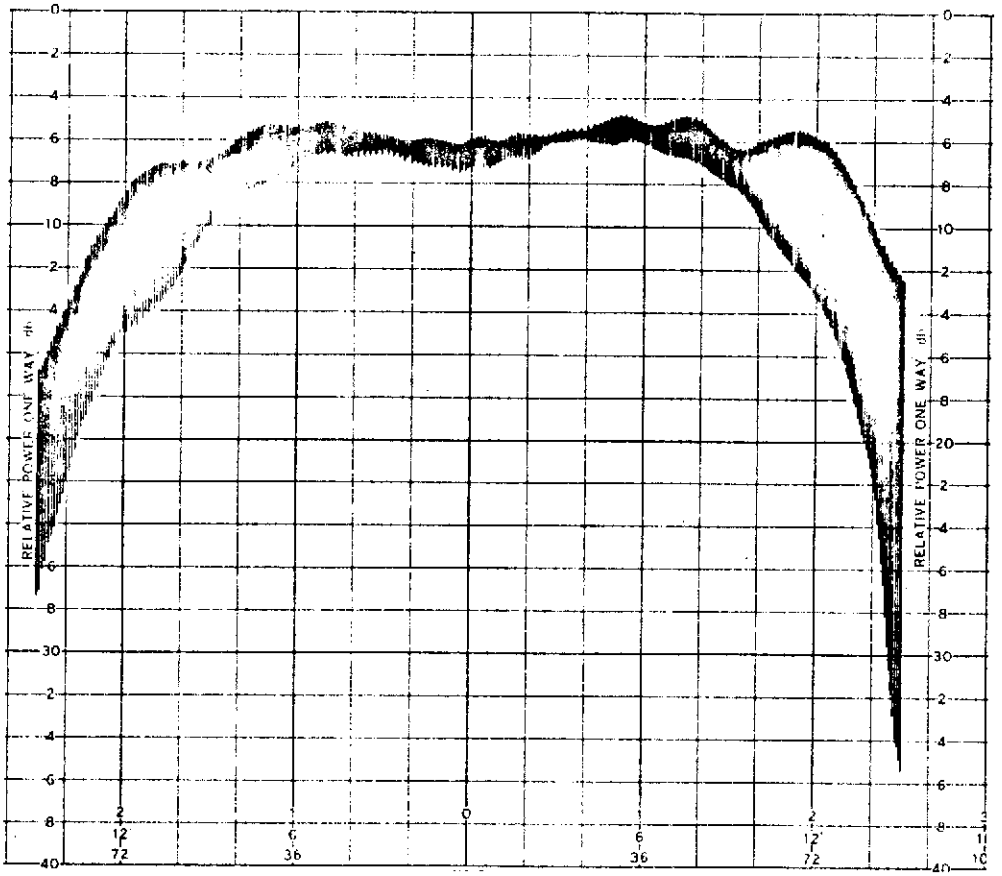


Figure 4-21. SPACS I Central Element S-Band Patterns In Array

Central Element Pattern, 2041.9 MHz,
ϕ=90° Cut From Elements 5 and 6
Toward Elements 1 and 2.

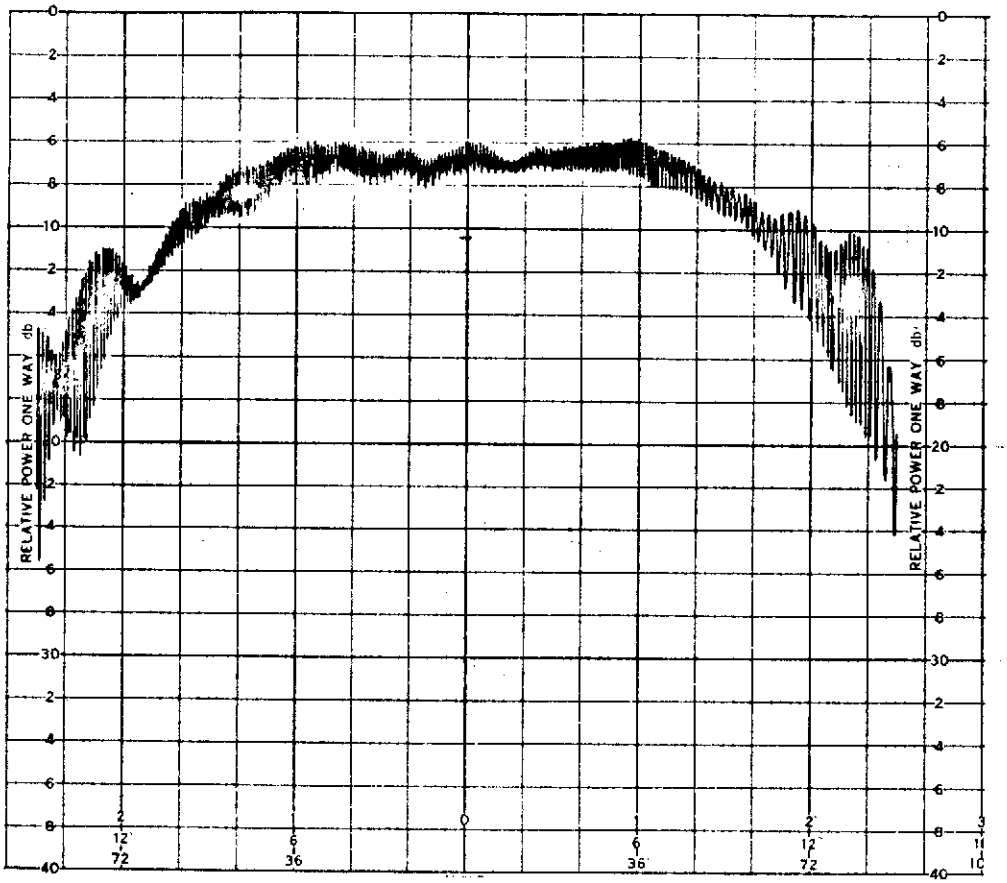


Figure 4-21. Continued

Central Element Pattern, 2106.4 MHz,
ϕ=0° Cut From Element 4 Toward
Element 3.

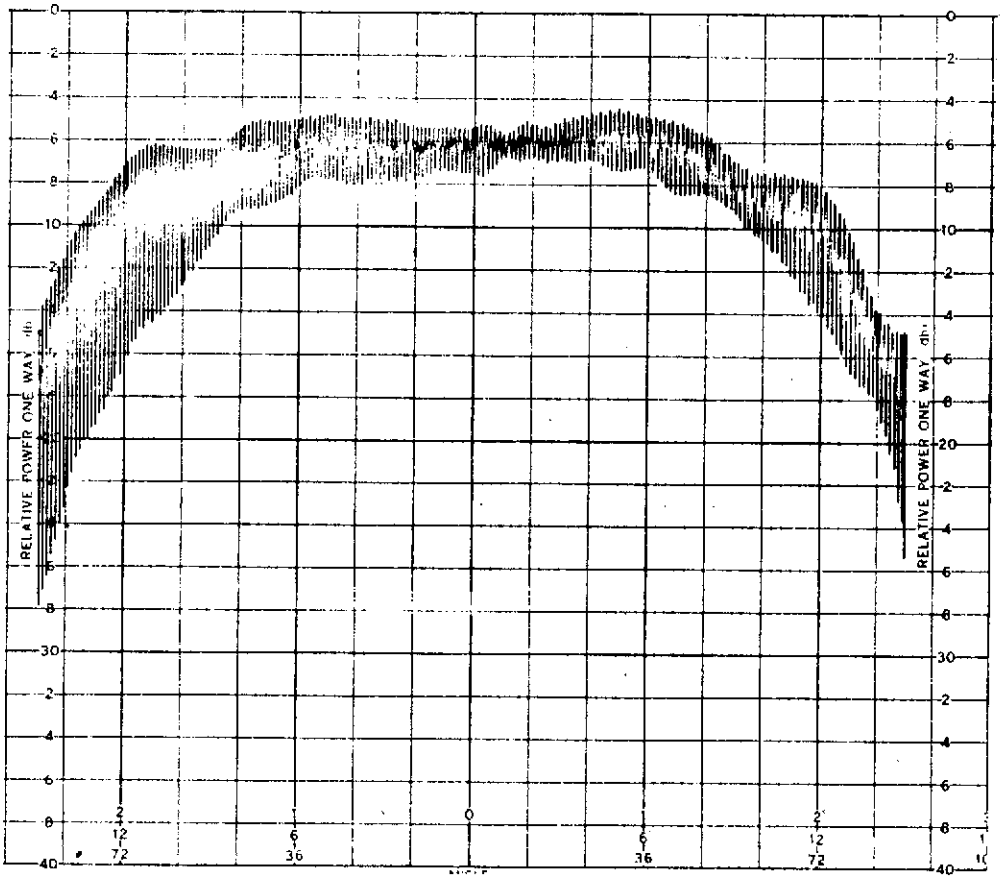


Figure 4-21. Continued

Central Element Pattern, 2106.4 MHz,
ϕ=90° Cut From Elements 5 and 6
Toward Elements 1 and 2.

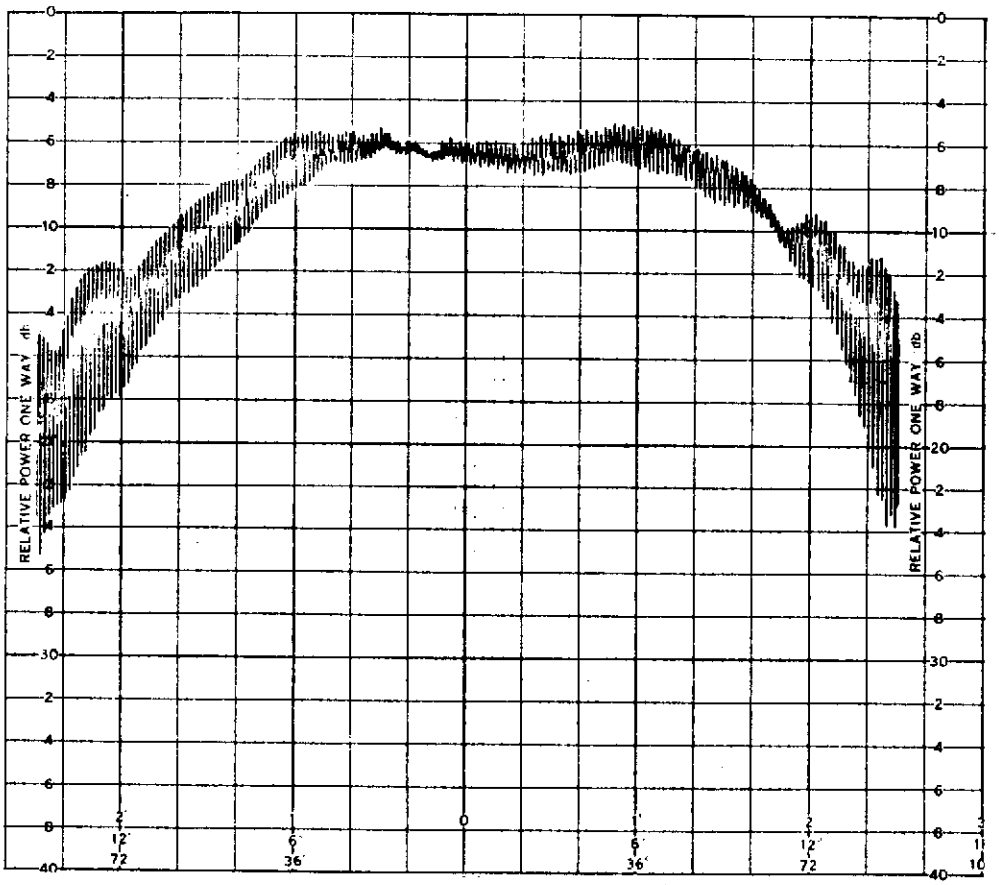


Figure 4-21. Continued

Central Element Pattern, 2217.5 MHz,
ϕ=0° Cut From Element 4 Toward
Element 3.

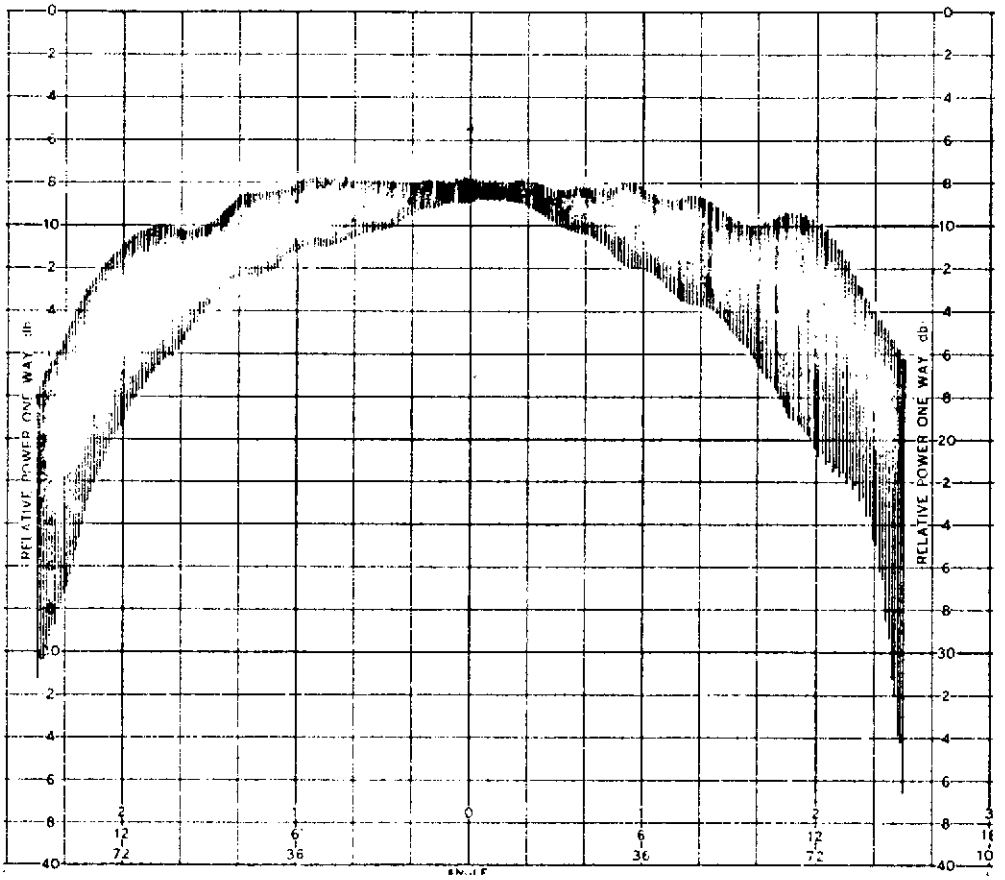


Figure 4-21. Continued

Central Element Pattern, 2217.5 MHz,
ϕ=90° Cut From Elements 5 and 6
Toward Elements 1 and 2.

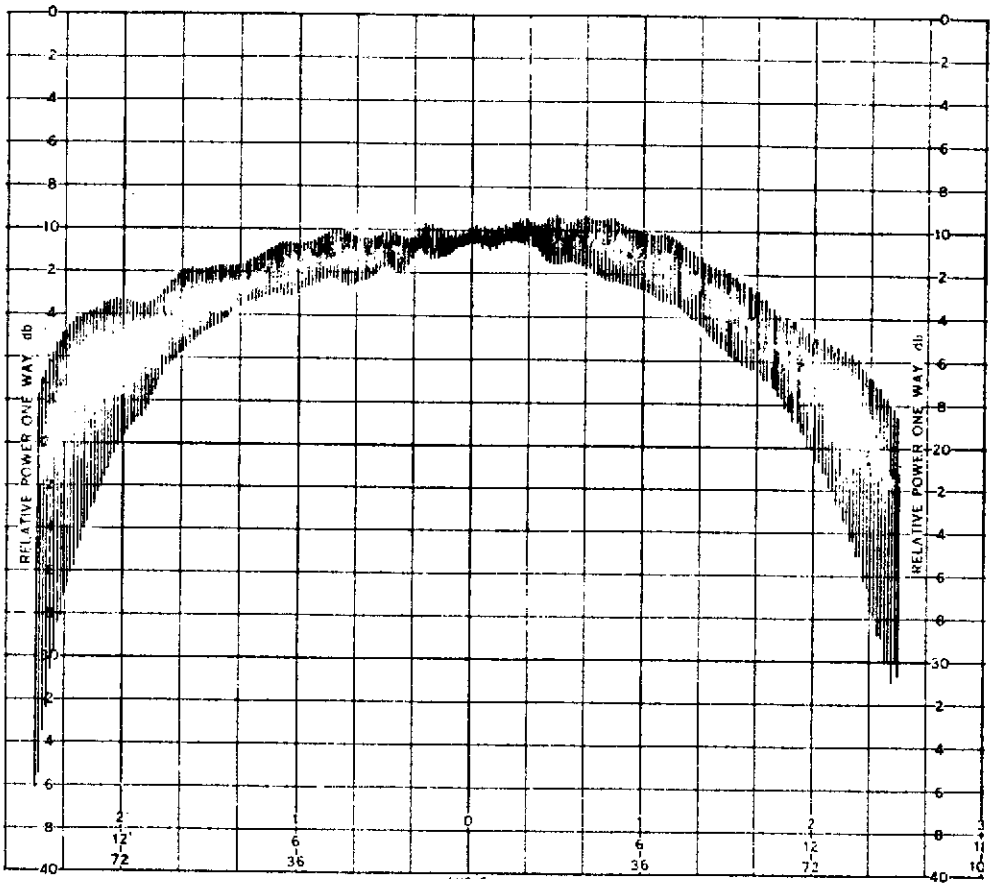


Figure 4-21. Continued

Central Element Pattern, 2287.5 MHz,
ϕ=0° Cut From Element 4 Toward
Element 3.

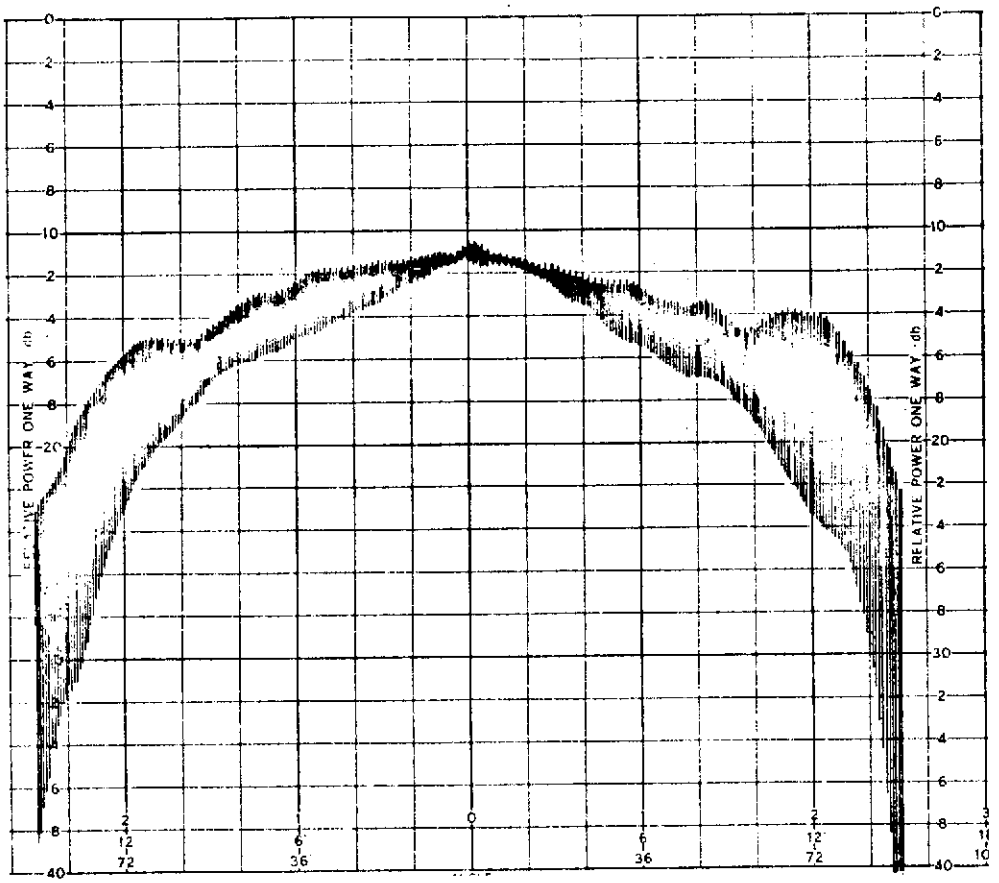


Figure 4-21. Continued

Central Element Pattern, 2287.5 MHz,
ϕ=90° Cut From Elements 5 and 6
Toward Elements 1 and 2.

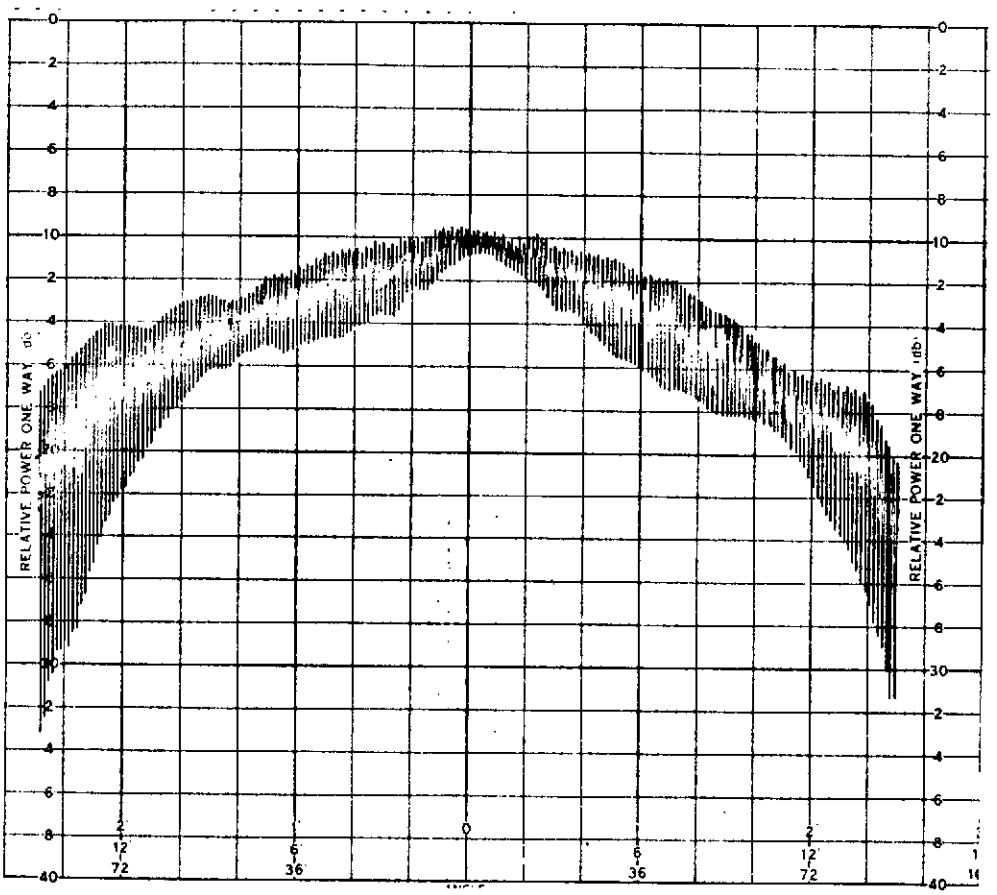


Figure 4-21. Continued

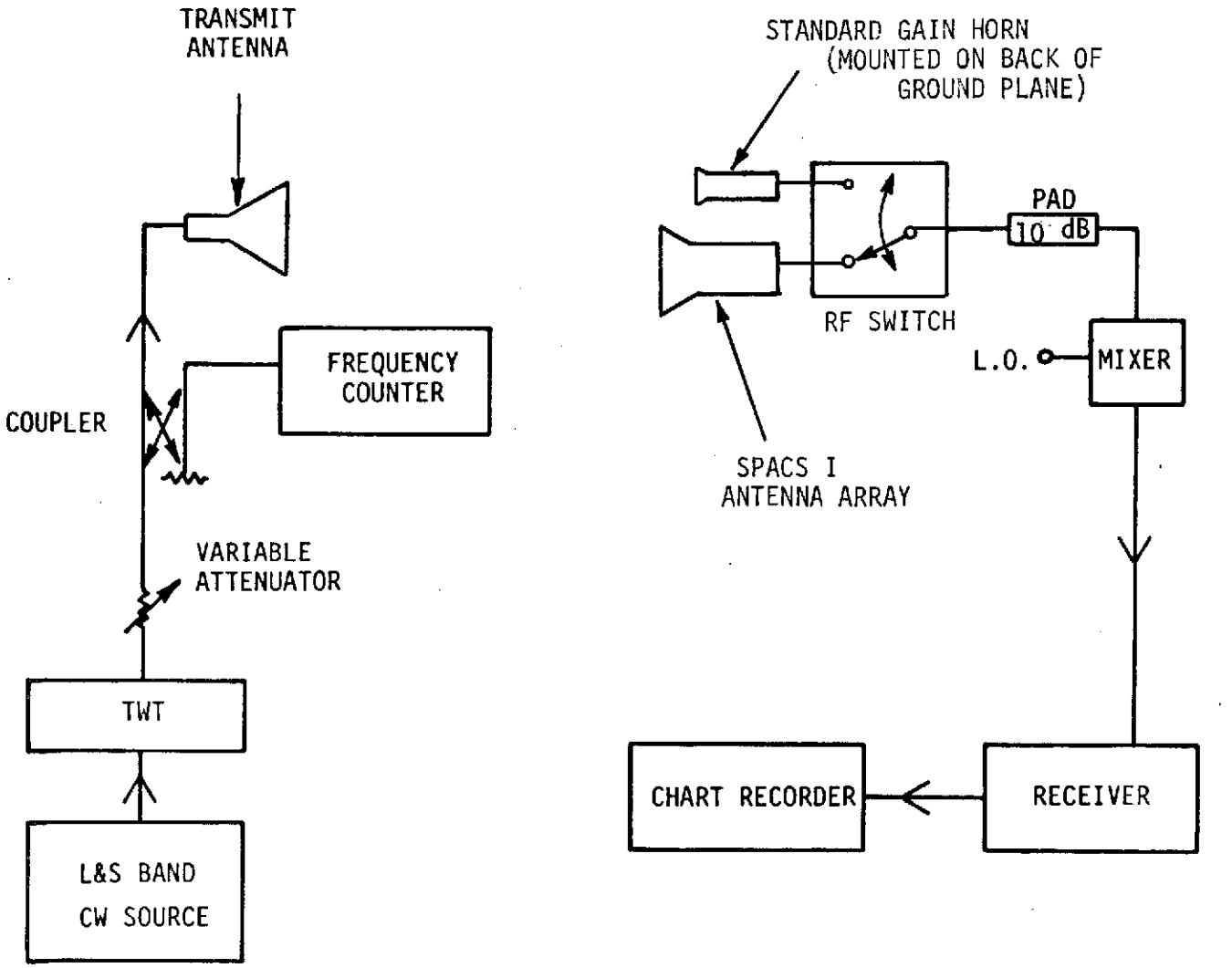


Figure 4-22. Gain Measurements

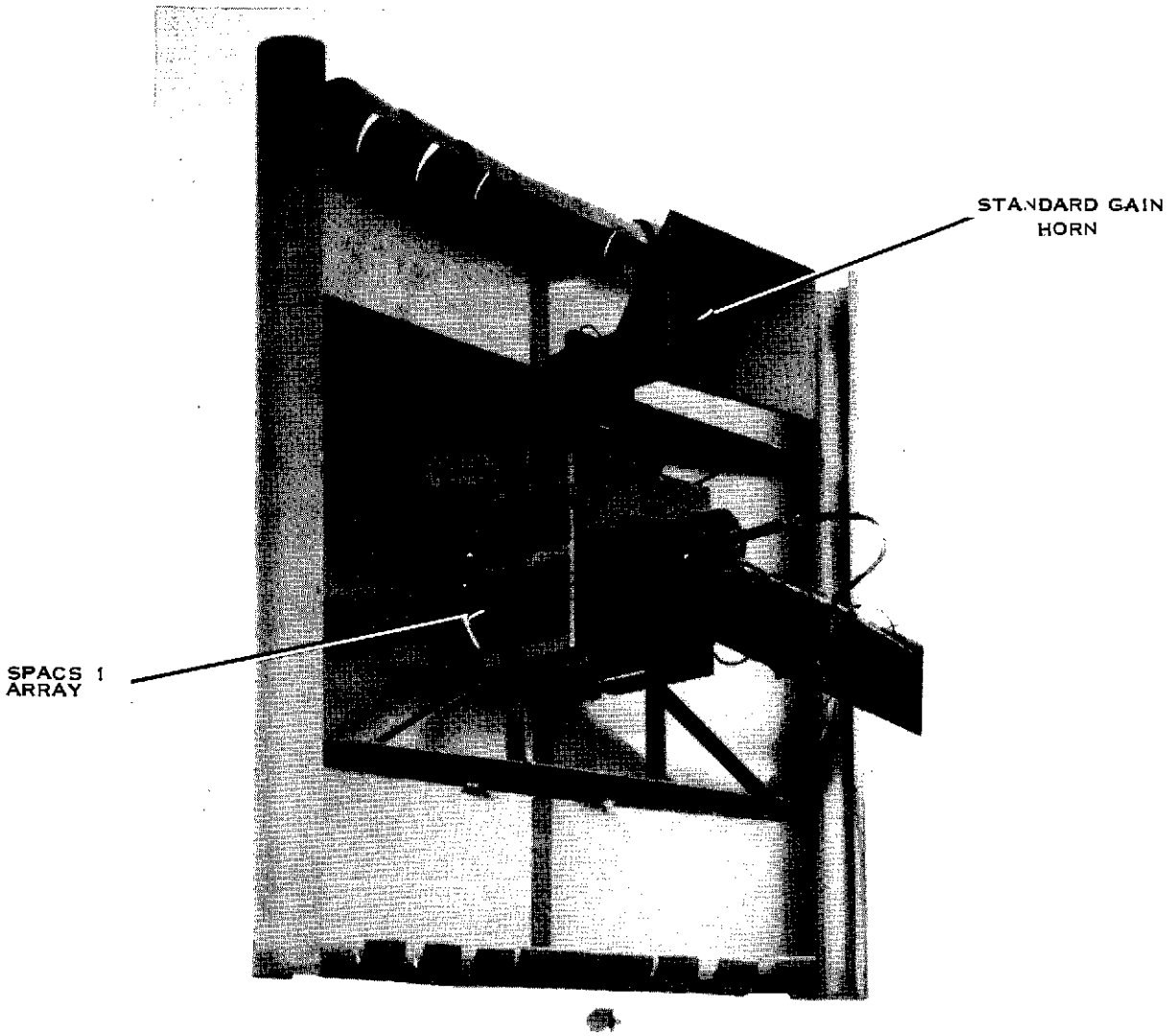


Figure 4-23. Back of SPACS I Array With Standard Gain Horn

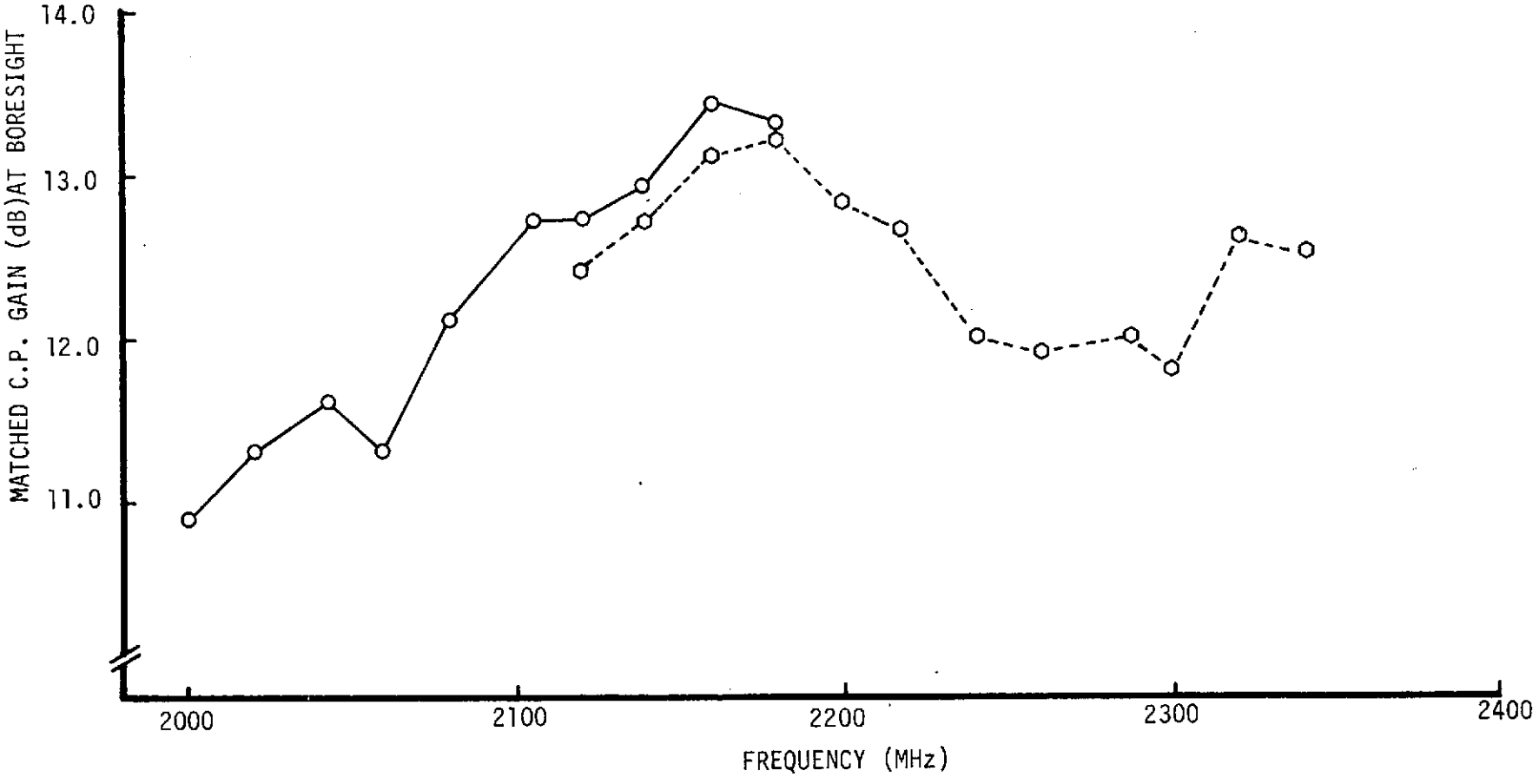


Figure 4-24. Array Boresight Gain

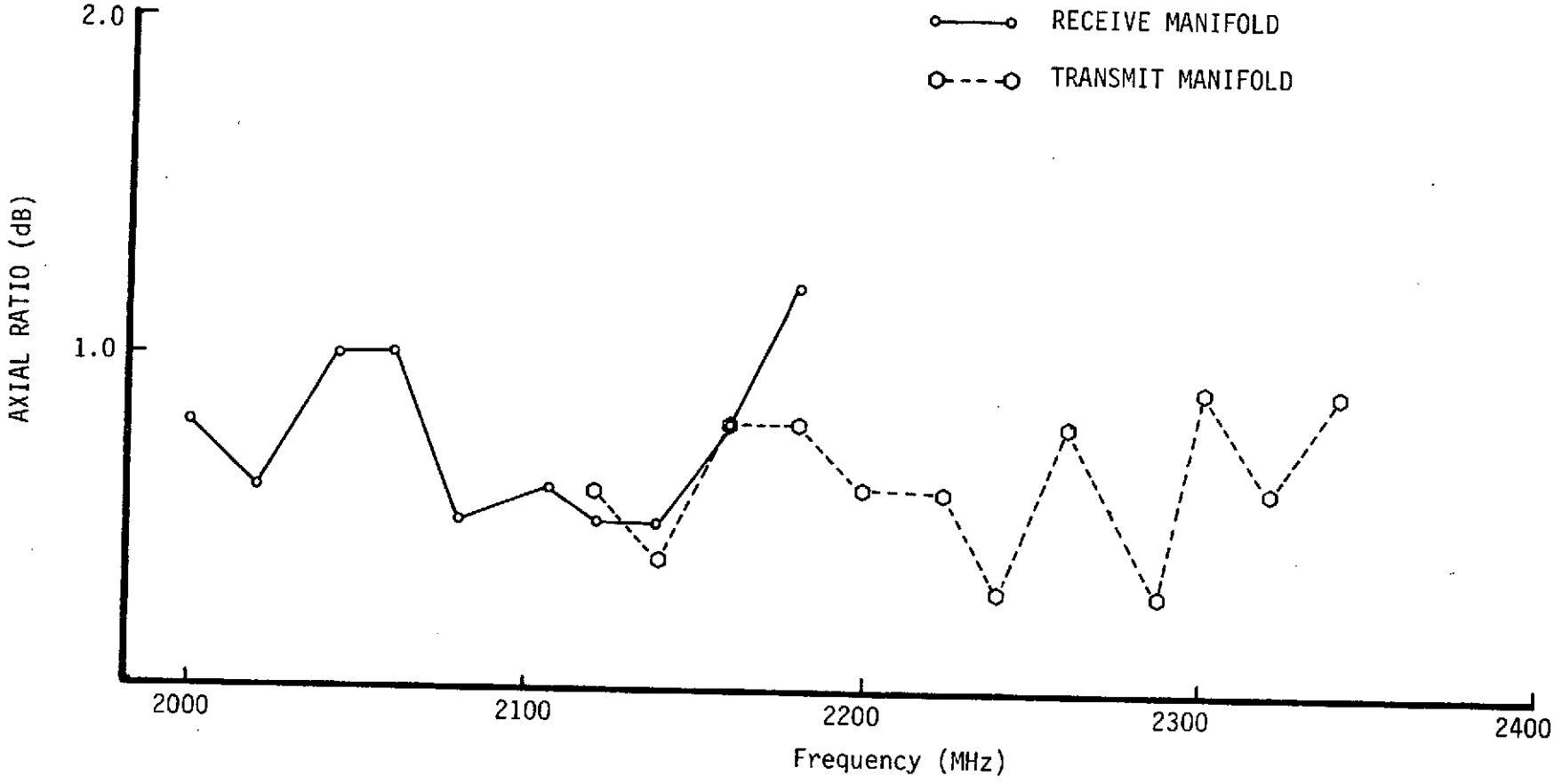


Figure 4-25. Array Axial Ratio (Boresight)

Figure 4-26 shows the gain at various angles when the beam was steered in both the roll plane and longitudinal plane. When comparing this data with the single element projections (Table 4-1), the 70° performance is better than expected; the 50° performance is lower than expected, and the 60° performance is as predicted. The differences are due primarily to mutual coupling. An examination of the central element pattern shows that the power does not roll off as fast at 70° as the isolated element. The 50° gain is lower in all probability due to grating lobe losses.

The axial ratio was approximately 1.5 dB at 50° scan (θ_o = 50°), 4.0 dB at 70° scan (θ_o = 60°), and 6.5 dB at 70° scan (θ_o = 70°).

The central element gain is shown in Figure 4-27. Since the element pattern dips slightly at boresight, the gain is defined to be the peak gain. The element gain is nominally 0 dB at the L-band frequencies. Figure 4-28 gives the axial ratio at this peak gain location as a function of frequency. The axial ratio is nominally 3 dB.

C. SUMMARY AND RECOMMENDATIONS FOR FUTURE IMPROVEMENT

A review of the breadboard array data shows that the overall performance is quite good. Of particular importance is that the 70° gain is greater than 5 dB over the S-band frequency range. A complete summary of tests and reduced test data is shown in Appendix A.

The balun board should be improved in future work. In general, we might expect that the engineering model results might be approached. The L-band performance can be improved by experimental studies on loading, cavity design, and balun design.

In future work, considerations should also be given to environmentally hardening the element. The twin coaxial transmission line between the balun and the spiral feed should be replaced with an etched dual microstrip line. This would substantially improve the mechanical properties. Additionally, foam loading of the cavities should be examined. This should also improve the mechanical properties of the spiral. With a proper selection of the foam, we might also improve the electrical performance.

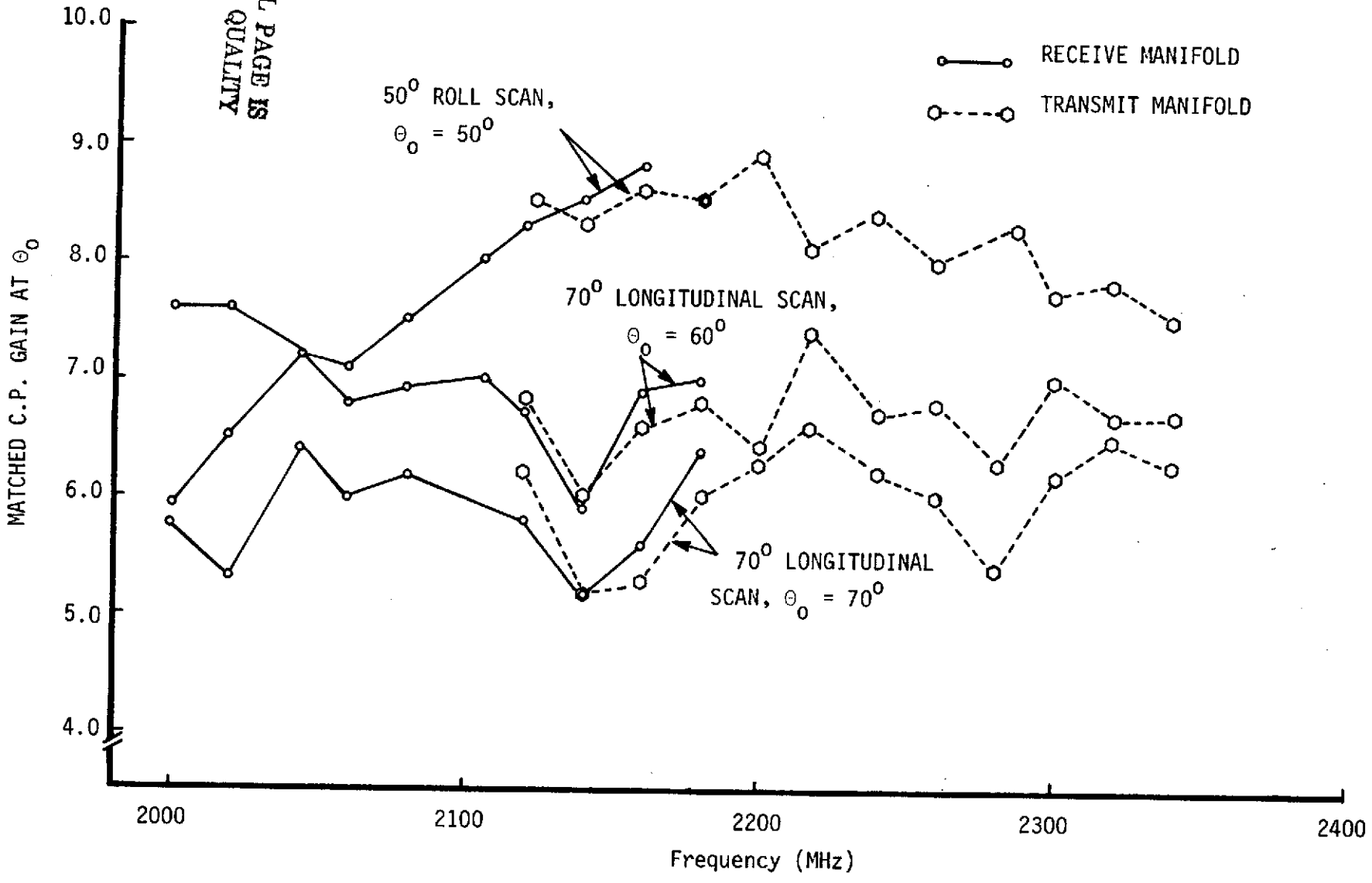


Figure 4-26. Array Gain With Scan

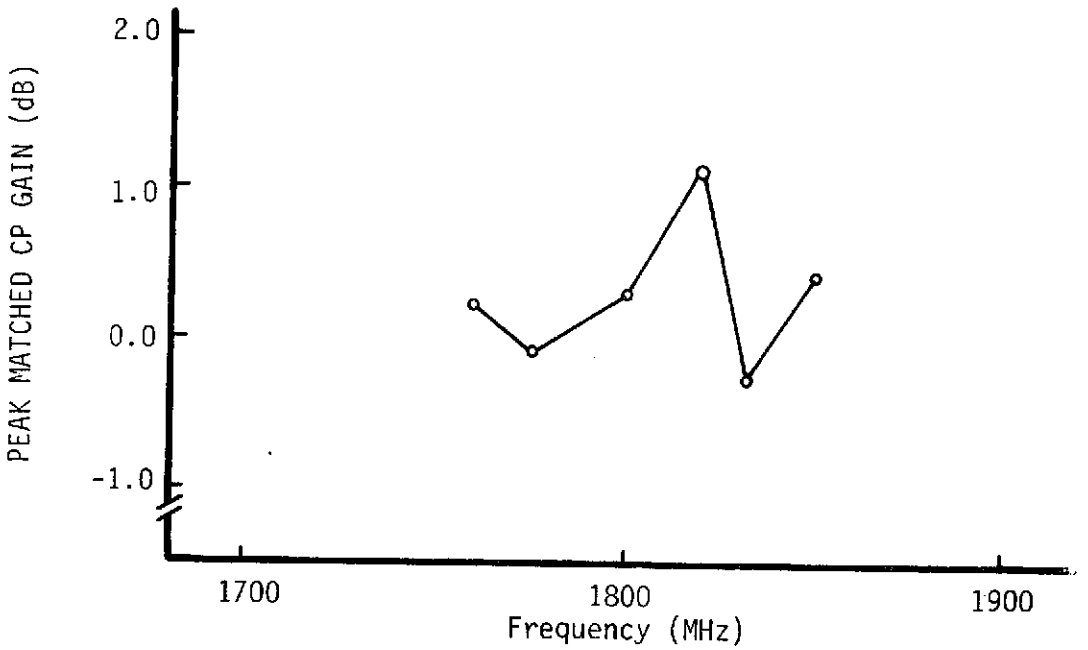


Figure 4-27. Central Element Gain

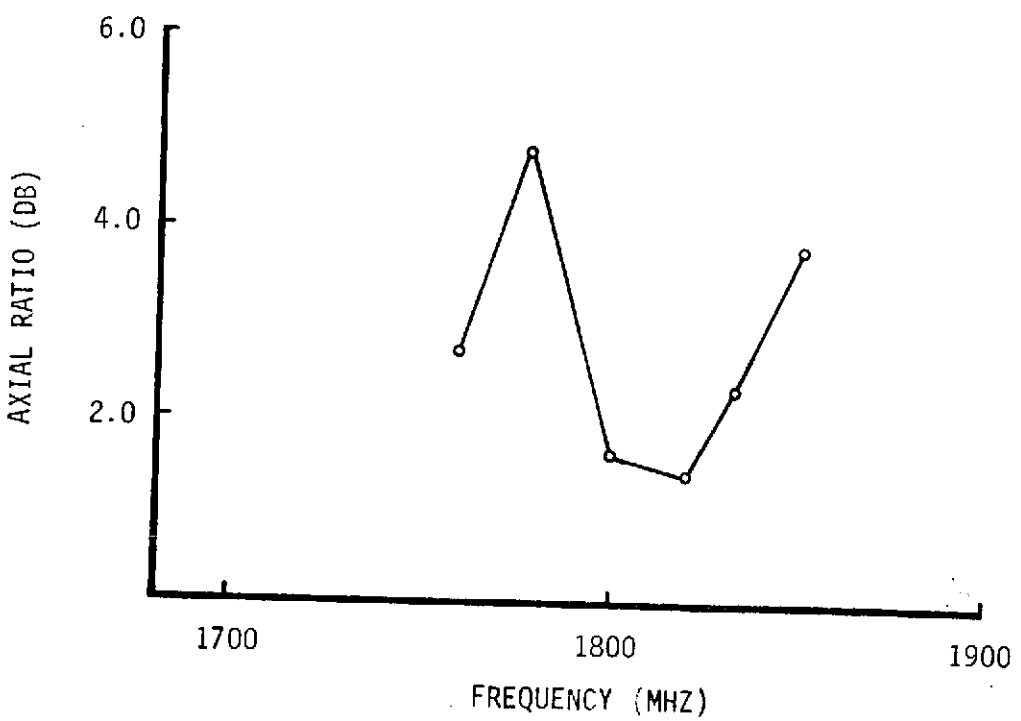


Figure 4-28. Central Element Axial Ratio

SECTION V

MODULE DESIGN AND EVALUATION

A. MODULE DESIGN

1. Transmit Phase Shifter Design

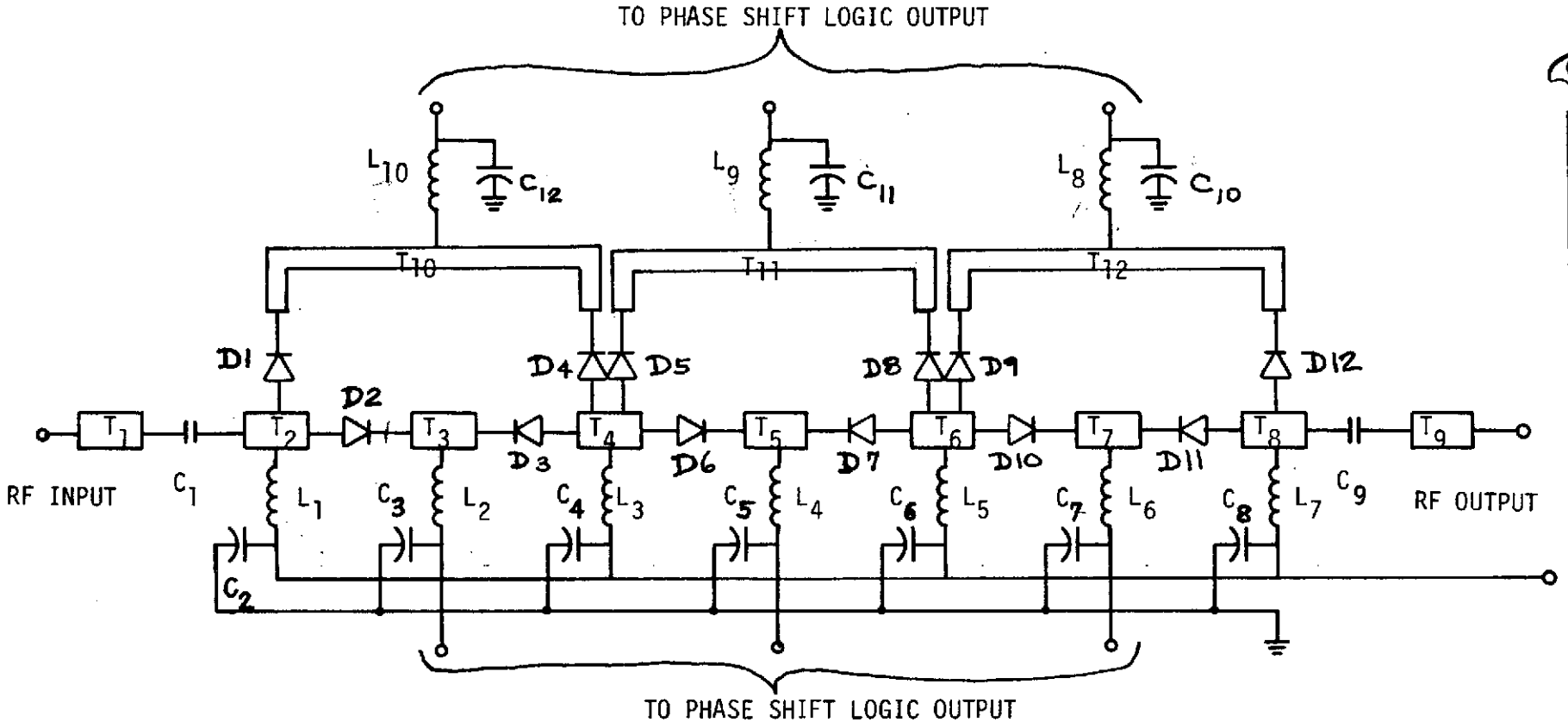
The electronic phase shift circuit utilized by the module transmitter is a 3-bit, line-length type phase shifter which utilizes thin-film microwave hybrid circuit techniques in its construction. In the line-length phase shifter, phase bits are realized by fixed segments of transmission line whose electrical lengths are established so as to represent a given value of phase shift at some reference frequency. In the case of the SPACS I module transmitter, these line lengths were designed for 45, 90, and 180 degrees of phase shift at 2252 MHz. These three primary phase bits are selectively switched into the signal transmission path to achieve differential phase shift from 0 to 315 degrees in 45 degree increments.

All line switching is achieved through the use of beam lead step recovery diodes shown schematically in Figure 5-1. In the "on" state (forward bias) this diode type has a relatively low dynamic resistance and minimizes the phase shifter insertion loss. Since one diode pair of each phase bit is always in the transmission path (6 diodes total in this case), use of higher resistance diodes can result in significant increases in phase shifter insertion loss.

Data shown in Table 5-1 compares the performance of a particular phase shifter fabricated initially with PIN diodes (chip components) with that of the same phase shifter circuit fabricated with step-recovery diodes (beam-lead components). Note that insertion loss ranges from 4 - 5 dB when using PIN diodes (chip) compared to 2 - 2.5 dB when using step-recovery beam lead diodes. Input VSWR improves from a range of 1.2:1 - 1.8:1 to 1.1:1 - 1.4:1 as the chip diodes and their associated inductive connections (bond wires) are replaced by the lower inductance beam lead components.

A comparison of phase errors for the same phase shift network using chip or beam lead components is shown in Table 5-2. Note that phase errors tend to accumulate as the higher bit positions are switched in, though not as rapidly once the chip components are replaced by beam lead components.

The basic phase shifter configuration used for the SPACS module was first demonstrated in the AESPA module (Contract No. NAS8-25847, Marshal Space Flight Center). This circuit was reconfigured with minor



T_1-T_8 : Microstrip transmission lines, Z_0 = 50Ω, arbitrary length

T_9 : Microstrip tranmission line, Z_0 = 50Ω, miminum length 14.4° @ 2252 MHz, maximum length 108° @ 2252 MHz (analog phase trim)

T_{10} : Microstrip transmission line, Z_0 = 50Ω, BL = 180° @ 2252 MHz

T_{11} : Microstrip transmission line, Z_0 = 50Ω, BL = 90° @ 2252 MHz

T_{12} : Microstrip transmission line, Z_0 = 50Ω, BL = 45° at 2252 MHz

C_1-C_{12} : 150 pf

L_1-L_{10} : RF Choke (high-impedance microstrip meander line)

Figure 5-1. Schematic, Transmit Phase Shifter

	INSERTION LOSS		VSWR	
BIT	CHIP COMPONENTS	BEAM-LEAD COMPONENTS	CHIP COMPONENTS	BEAM-LEAD COMPONENTS
0	4.79 dB	2.43 dB	1.769	1.382
1	4.11	2.21	1.115	1.366
2	5.31	1.99	1.364	1.218
3	4.59	2.60	1.598	1.308
4	5.15	2.15	1.376	1.133
5	4.34	2.23	1.362	1.193
6	5.05	2.09	1.726	1.234
7	4.37	2.35	1.224	1.287

Frequency = 2280 MHz

TABLE 5-1. PHASE SHIFTER PERFORMANCE, INSERTION LOSS AND VSWR AS A FUNCTION OF COMPONENT TYPE

Table 5-2. Phase Shifter Performance, Phase Errors As A Function of Component Type

	Δ PHASE SHIFT (DEGREES)[1]				PHASE ERROR (DEGREE)			
		CHIP CONFIGURATION		BEAM LEAD CONFIGURATION		CHIP CONFIGURATION		BEAM LEAD CONFIGURATION	
BIT	REQUIRED	2220 MHz	2295 MHz	2220 MHz	2295 MHz	2220 MHz	2295 MHz	2220 MHz	2295 MHz
0	0								
1	-45	-41.3	-42.5	-48.2	-50.8	+ 3.7	+ 2.5	- 3.2	- 5.8
2	-90	-81.7	-83.8	-81.7	-84.0	+ 8.3	+ 6.2	+ 8.3	+ 6.0
3	-135	-120.3	-123.5	-128.4	-133.8	+14.7	+11.5	+ 6.6	+ 1.2
4	-180	-169.6	-174.3	-173.5	-179.5	+10.4	+ 5.7	+ 6.5	+ .5
5	-225	-207.9	-213.7	-219.5	-227.2	+17.1	+11.3	+ 5.5	- 2.2
6	-270	-244.9	-253.3	-250.5	-258.6	+25.1	+16.7	+19.5	+11.4
7	-315	-284.9	-296.6	-296.9	-307.8	+30.1	+18.4	+18.1	+ 7.2

[1] All values for bits 1-7 are referenced to the absolute phase shift recorded for the 0 bit at the given frequency.

changes to accept the beam lead diodes and capacitors, to conform to the inherent physical requirements of the SPACS module, and to be optimum for the center frequency (2252 MHz) of the SPACS transmit bandpass. Actual performance data recorded on the transmit phase shifter integrated into the breadboard module is shown in Table 5-3.

Circuit physical size is 0.600 x 1.150 inches on 0.025-inch thick alumina substrate material. All printed circuit elements are microstrip-type which are photolithographically defined, etched, and plated to desired thickness (typically 250 μ inches). Scribing to finished size and selective hole-drilling for feed-through grounding are accomplished through the use of numerically controlled laser equipment.

2. Power Amplifier Design

The original concept for the power amplifier configuration is shown in Figure 5-2. The first stage utilizes an MSC 80264 transistor operating in the common emitter Class A mode. The second stage utilizes an MSC 4001 transistor operating self-bias (Class C) in the common base mode. The third stage utilizes an MSC 2023-6 AMPAC device which is internally matched for Class C operation (common base) in a 50-ohm system.

Characterization of each device was performed and results are shown in the following tables and figures. S-parameters for the MSC 80264 are shown in Table 5-4; compression characteristics of the device are shown in Figure 5-3. S-parameters were measured on this device at input levels of +12 dBm using the Hewlett-Packard Automatic Network Analyzer and high power hardware/software developed by Texas Instruments Inc., Advanced Systems Department. The MSC 4001 was characterized at V_{cc} levels of 20, 22, and 24 volts with an RF input level of 0.1 watts. Typical performance characteristics are shown in Figure 5-4. Large signal input and output admittances are shown in Figure 5-5. The MSC 2023-6 was also characterized at V_{cc} levels of 20, 22, and 24 volts with an RF input level of 1.2 watts. Typical operating characteristics are shown in Figure 5-6 Input impedance of the internally matched device is nominally 50 ohms; large-signal output impedances are shown in Figure 5-7.

Prior to initiating circuit designs based upon the above data, a critique of the design requirements and hardware delivery schedule indicated that some commonality existed between the AESPA module power amplifier (Contract No. NAS8-25847, Marshall Space Flight Center) and the SPACS power amplifier requirement. The SPACS power amplifier was then reconfigured to utilize the AESPA power amplifier as the first two stages preceding the MSC 2023-6 third stage; this configuration is shown in Figure 5-8.

Circuitry was assembled to evaluate this approach and results are shown in Figure 5-9. This configuration was subsequently modified to optimize the amplifier bias conditions. This configuration was integrated into the breadboard module and is shown schematically in Figure 5-10.

Table 5-3. Transmit Phase Shifter Performance, Breadboard Module

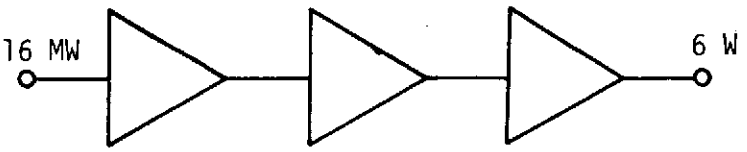
Bit	Commanded Phase (Degrees)	Insertion Loss (dB)	VSWR (Ratio)	Phase Error (Degrees)
0	0	1.82	1.362	-
1	45	1.75	1.282	- 2.4
2	90	1.69	1.499	- 2.6
3	135	2.10	1.705	- 8.4
4	180	1.57	1.067	- 0.3
5	225	1.60	1.130	- 5.2
6	270	1.58	1.206	- 6.2
7	315	1.97	1.381	-11.6

FREQUENCY = 2250 MHz

TABLE 5-4. S-PARAMETERS MSC 80264 TRANSISTOR

V_{ce} = 10V, I_c = 50 mA

FREQUENCY (MHz)	INPUT POWER LEVEL (dBm)	S_{11}		S_{21}		S_{12}		S_{22}	
		M	θ	M	θ	M	θ	M	θ
2000	6	.78	122°	1.46	-5°	.05	52°	.63	-114°
2250		.75	108°	1.35	-17°	.06	46°	.65	-121°
2500		.73	90°	1.31	-30°	.08	39°	.66	-125°
2000	12	.79	122°	1.47	-5°	.05	51°	.65	-113°
2250		.76	108°	1.35	-18°	.06	45°	.66	-121°
2500		.73	89°	1.31	-30°	.08	38°	.67	-125°
2000	18	.80	123°	1.36	-5°	.05	50°	.65	-113°
2250		.77	109°	1.27	-18°	.06	45°	.66	-121°
2500		.74	90°	1.24	-30°	.08	38°	.68	-125°



POWER GAIN (dB)	8	11	7
DEVICE TYPE	MSC80264	MSC4001	MSC2023-6
V_{cc}	+12VDC	+24VDC	+24VDC
OPERATING CURRENT (mA)	50	100	500

Figure 5-2. Power Amplifier Configuration, Original Concept

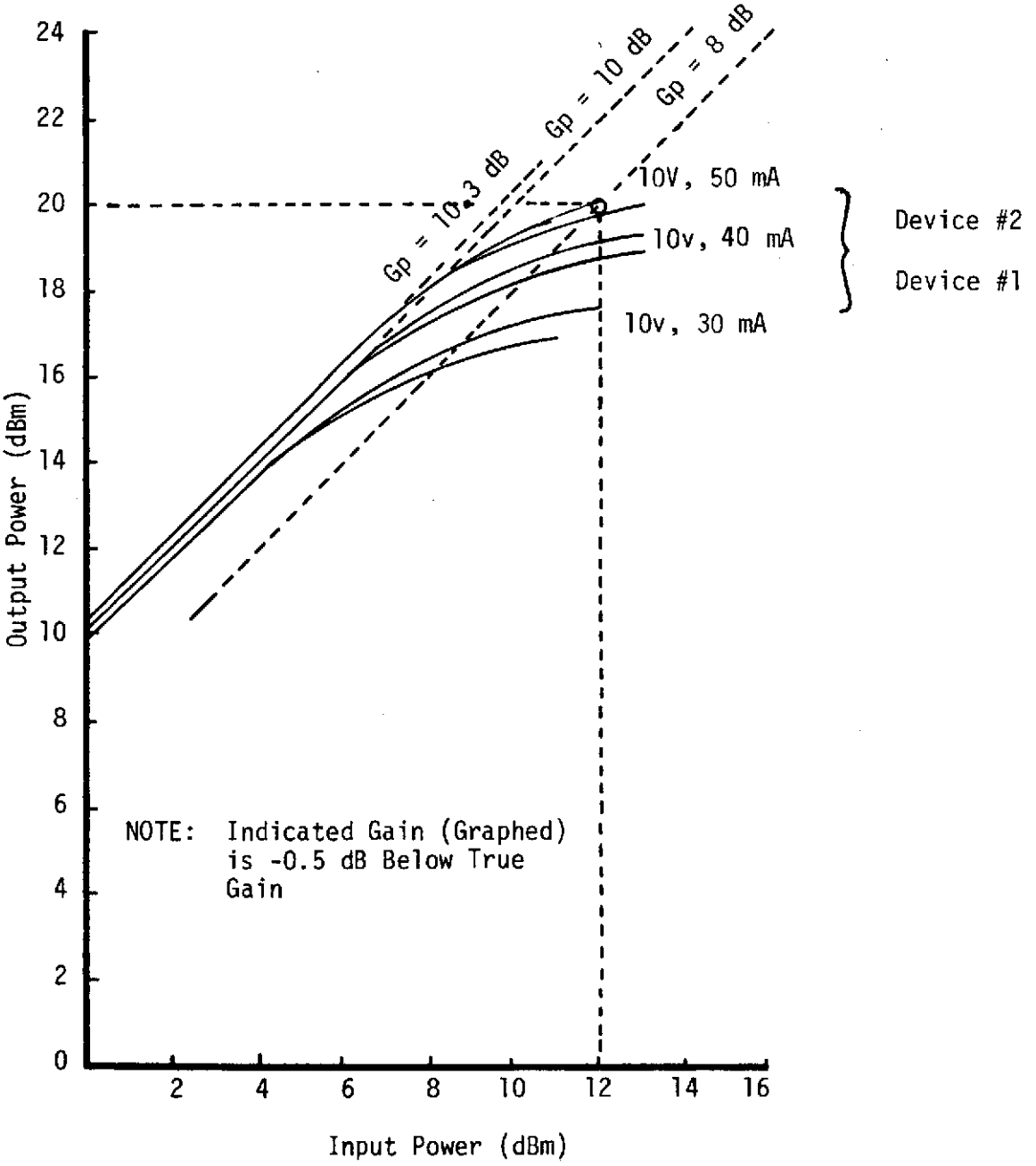


Figure 5-3. Gain Compression Characteristics, MSC 80264 Transistor

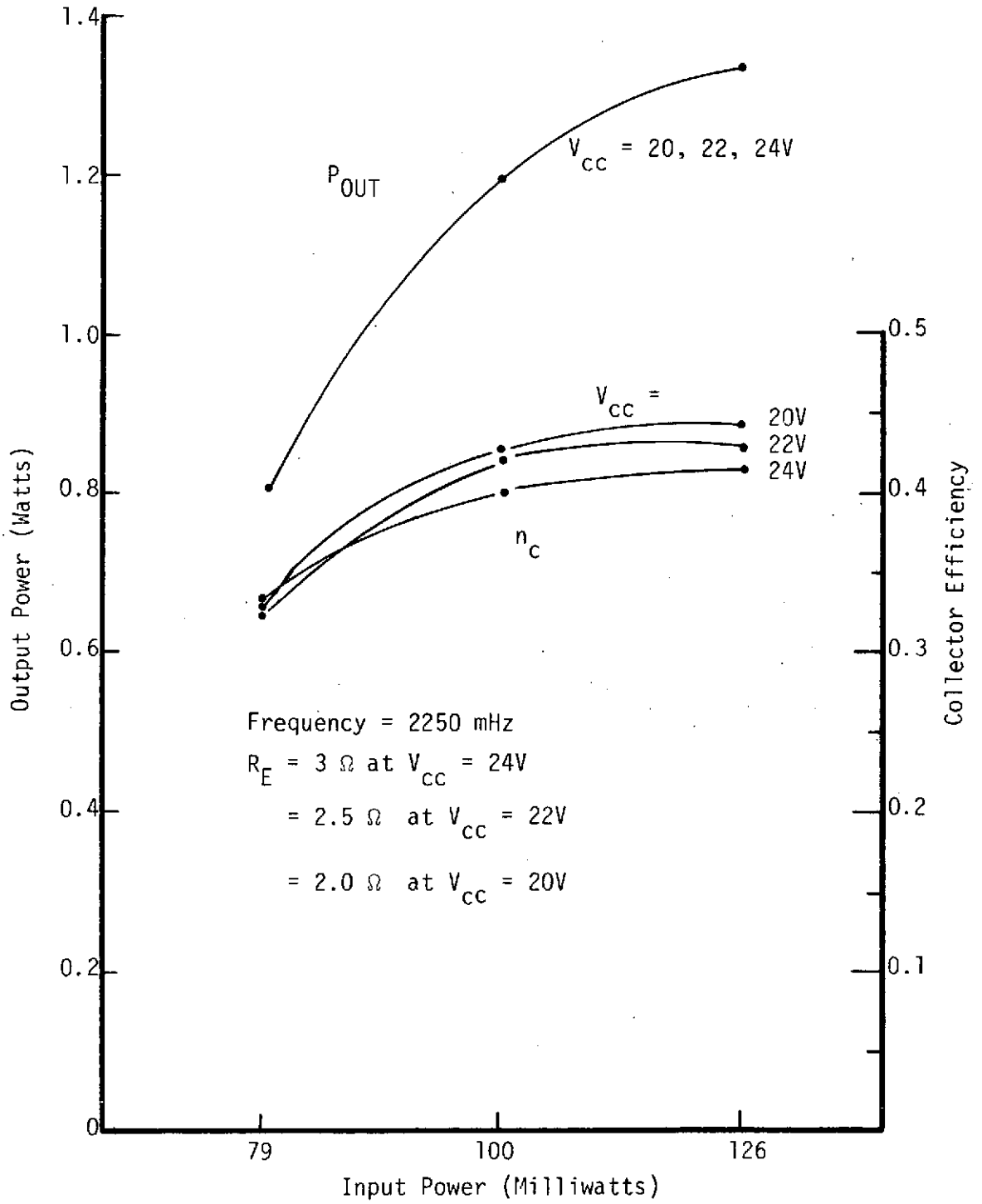


Figure 5-4. Large-Signal Operating Characteristics, MSC 4001 Transistor

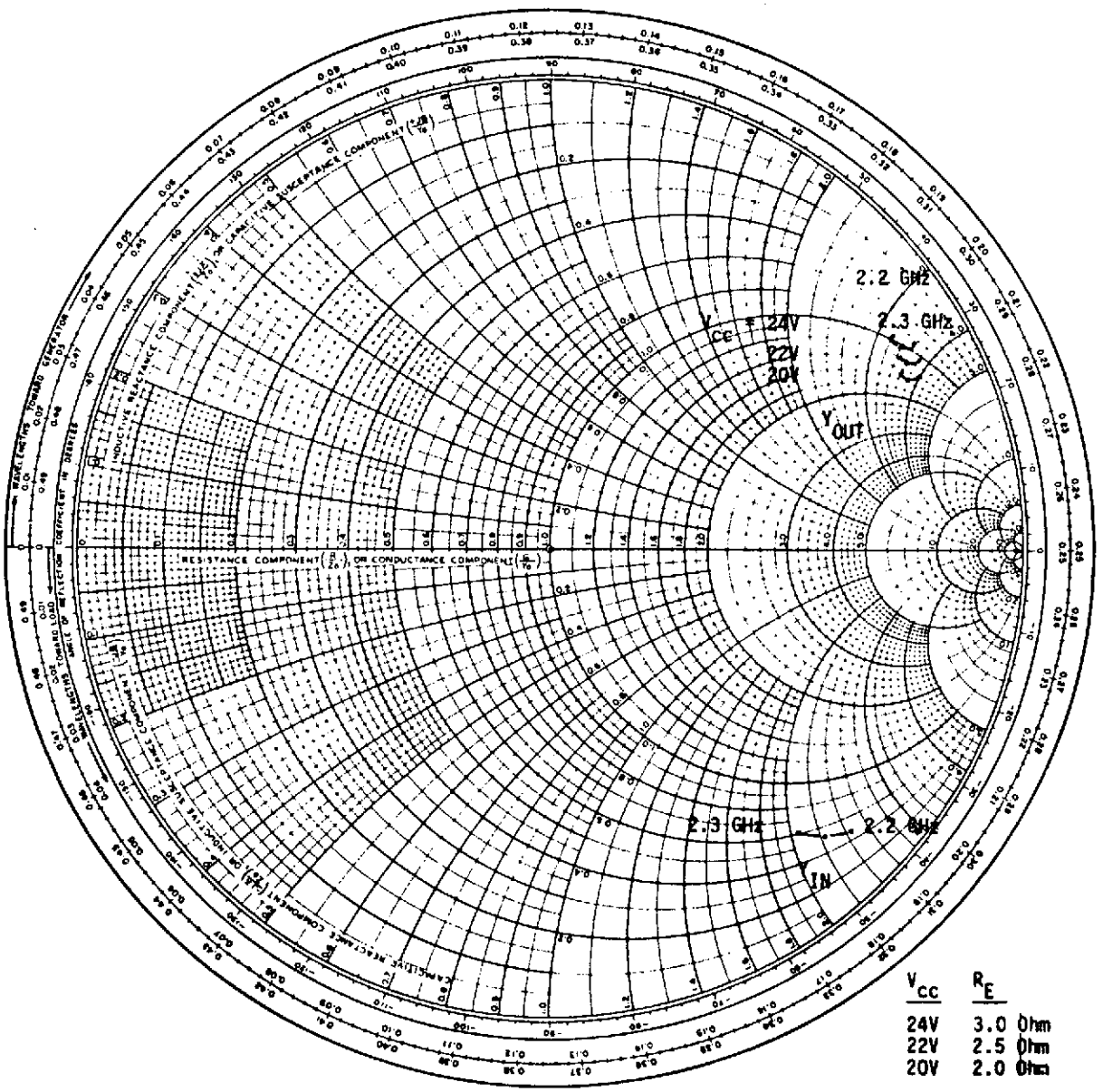


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Figure 5-5. Optimum Device Admittances, MSC 4001, Large-Signal Operation, Gain = 10.8 dB

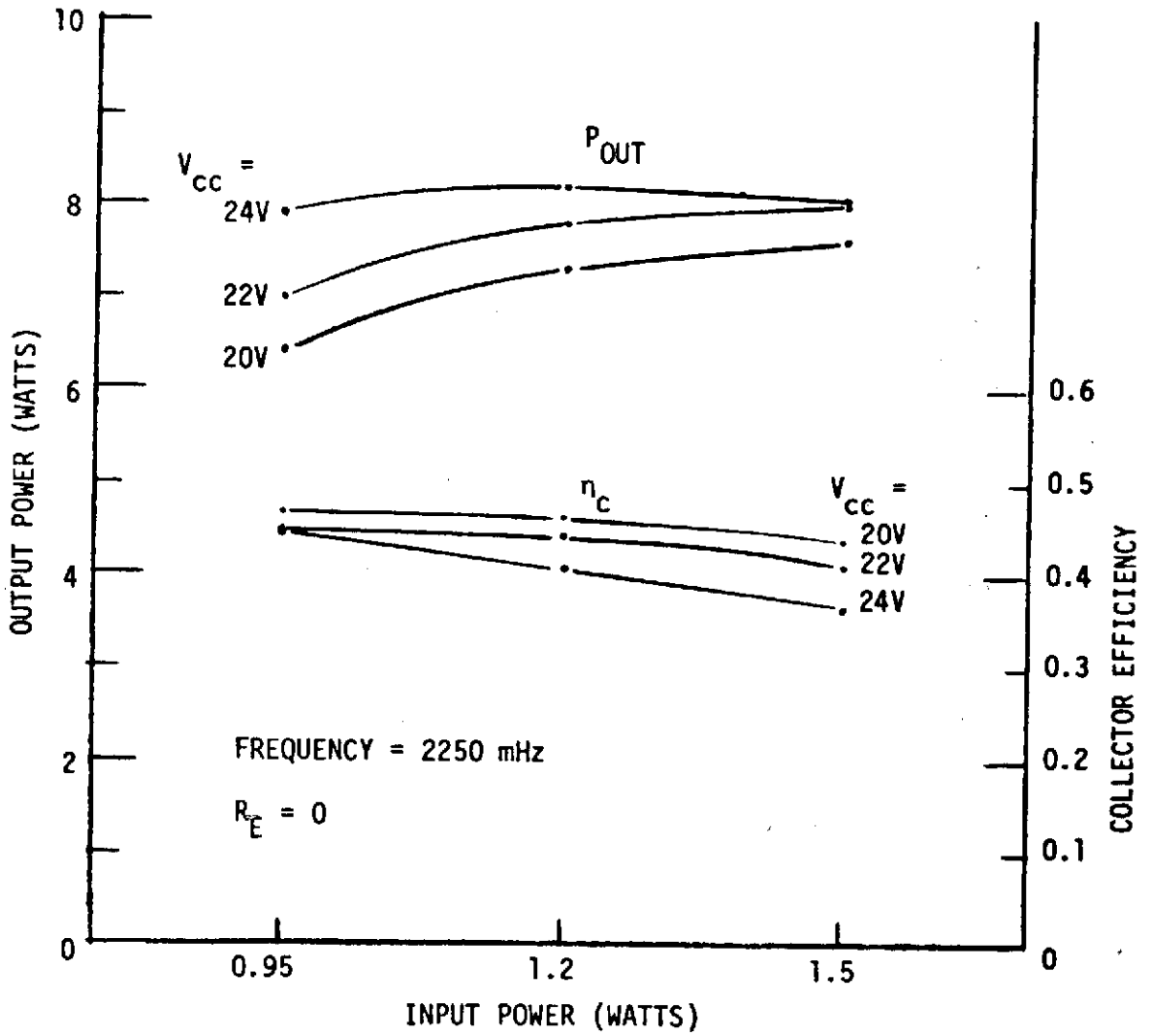

Figure 5-6. Large-Signal Operating Characteristics, MSC 2023-6 Transistor

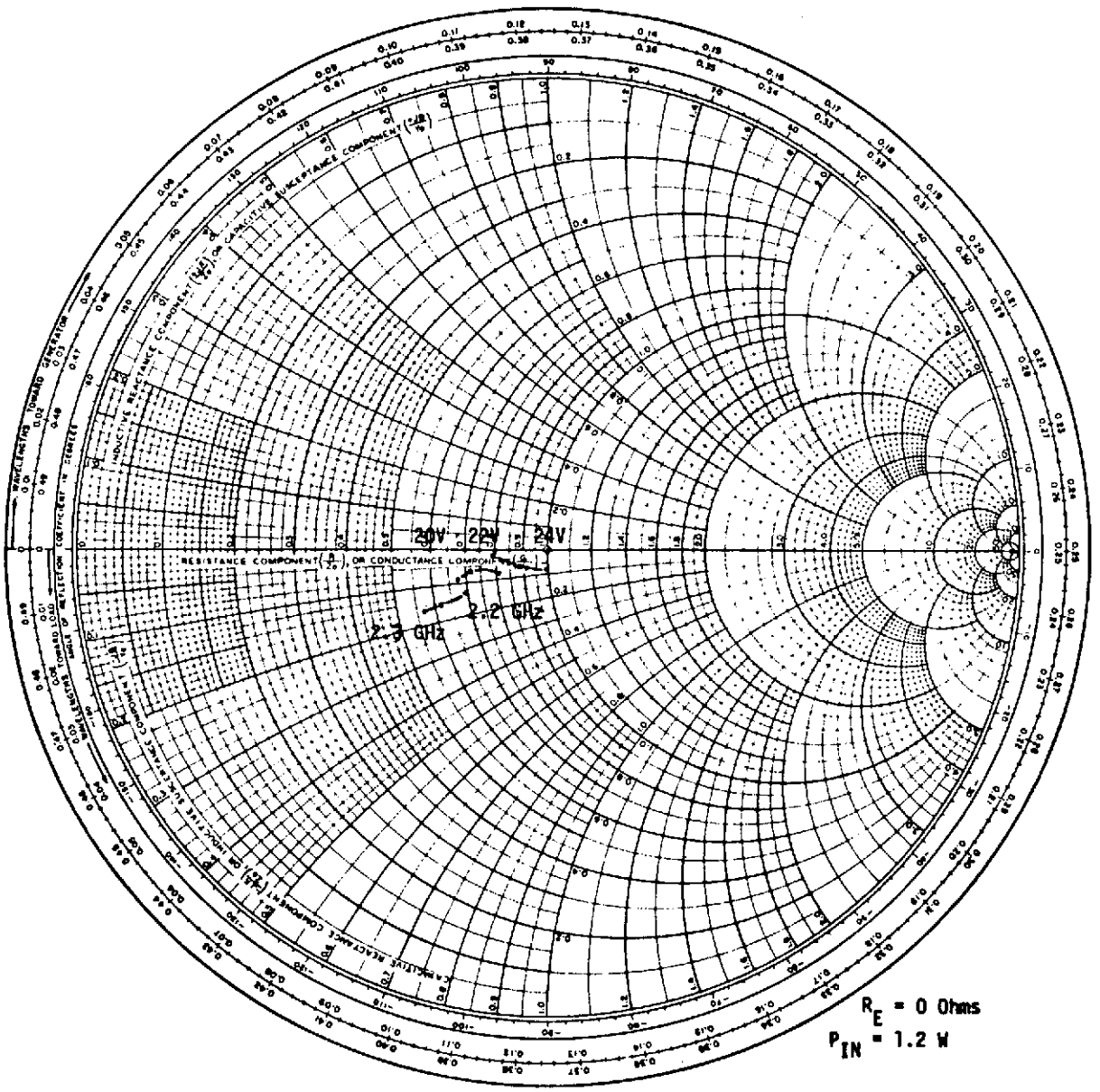

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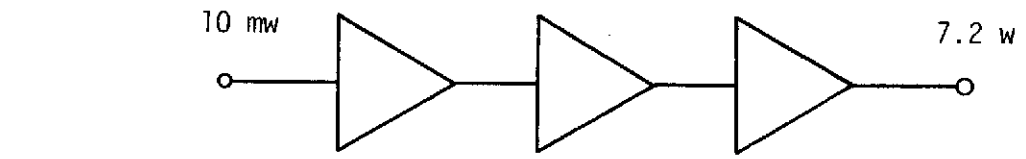
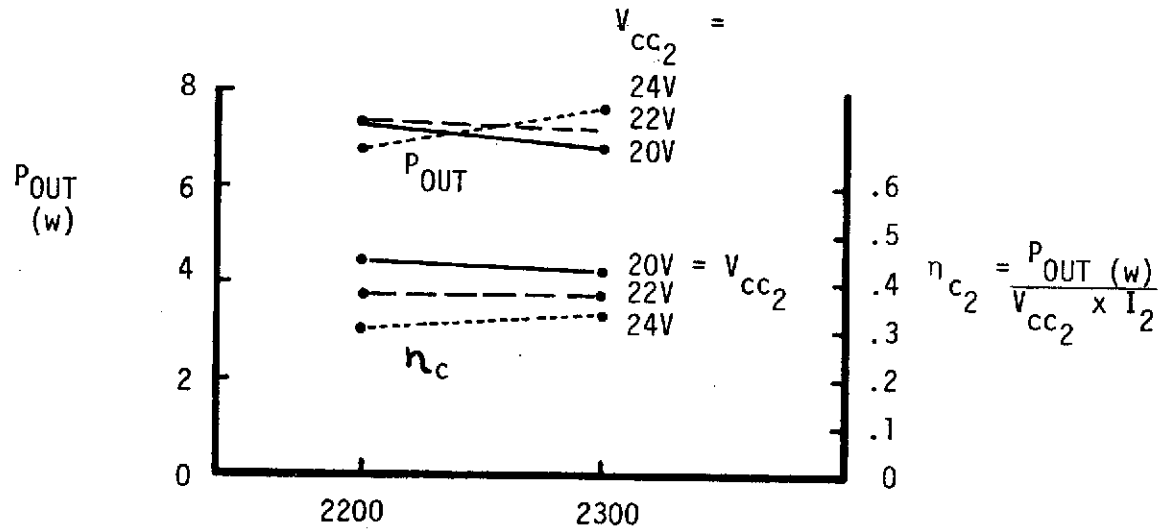
Figure 5-7. Optimum Collector Load Impedance, MSC 2023-6 Transistor, Gain = 7.8 - 8.3 dB



Power Gain (dB)	9.8	11	7.8
Device Type	MS251	MSC4001	MSC2023-6
V_{cc}	+22VDC	+22VDC	+22VDC
V_{BB}	+12VDC	N.A.	N.A.
Operating Current (mA)	26 mA	120 mA	750 mA

Figure 5-8. Power Amplifier, Breadboard Configuration



P_{in} = 20 mw (+13 dBm)

V_{cc_1} (1st and 2nd stages) = 20 VDC

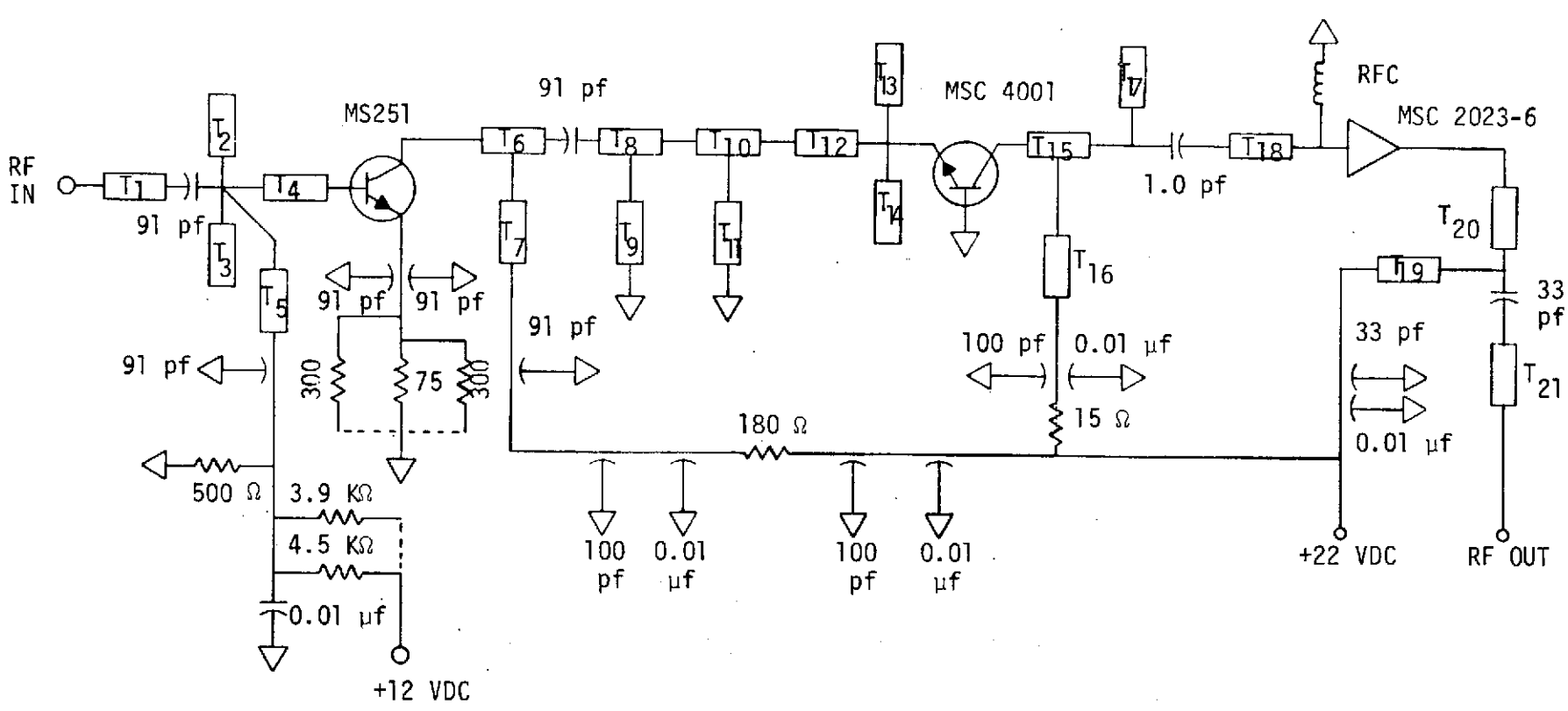
I_1 (1st and 2nd stages) = 150 mA (Typ)

V_{cc_2} (3rd stage) = 20-24VDC

I_2: 3rd stage current only

η_{c_2}: 3rd stage collector efficiency

Figure 5-9. Breadboard Power Amplifier Performance



T_1 - T_{21} : Microstrip Transmission Line Elements

T_2, T_3, T_{13}, T_{14}, T_{17}; open stubs

T_9, T_{11}; shorted stubs

T_5, T_7; high impedance meander lines (rf chokes)

T_{16}, T_{19}; high impedance, $\lambda/4$ lines (rf chokes)

RFC: 6.5 Turns on a 0.025" form

Figure 5-10. Schematic, Breadboard Power Amplifier

3. Transmit Filter Design

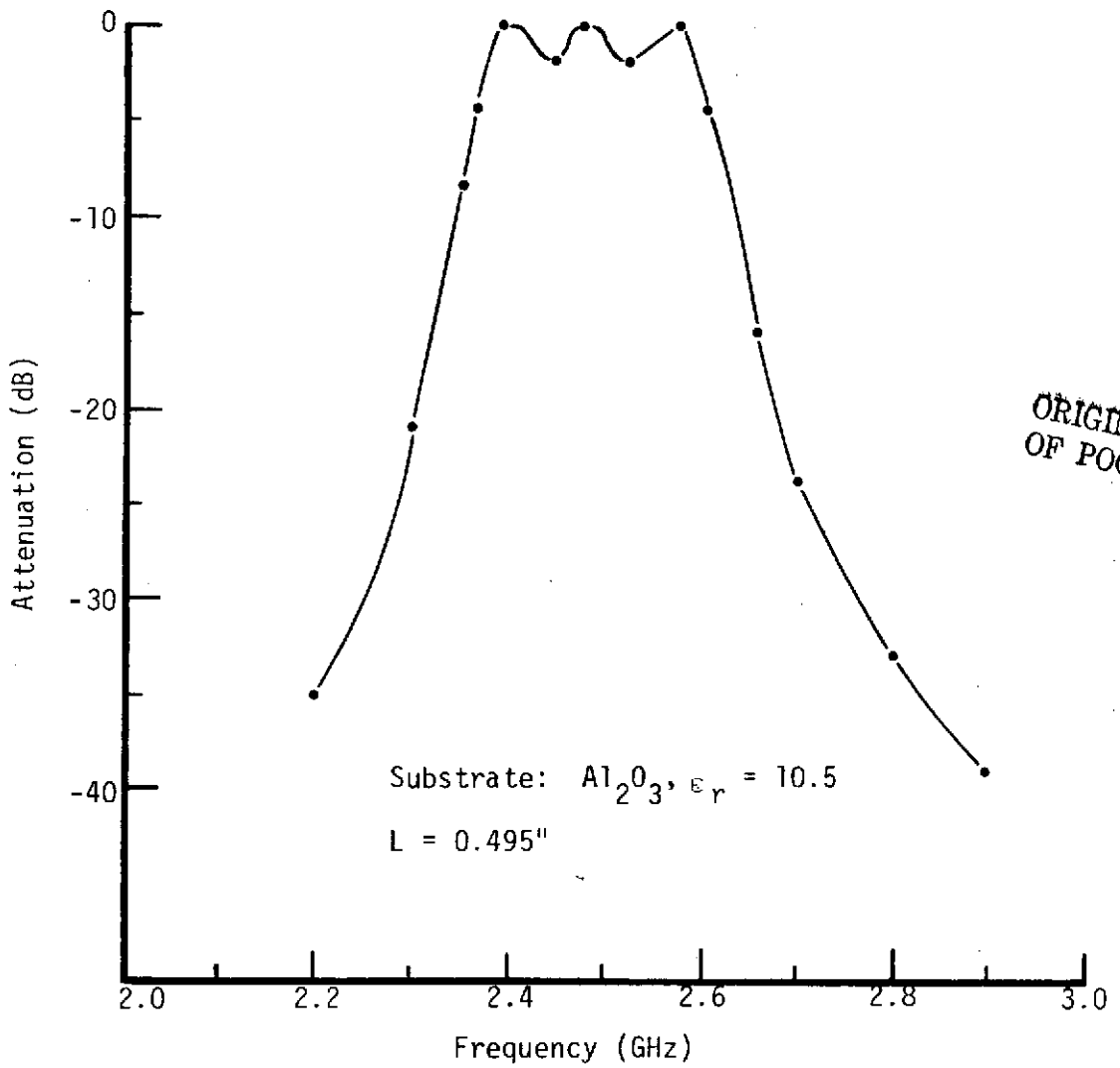
Bandpass filtering of the module transmitter was originally established as a prime requirement for the SPACS I array. Frequency rejection and in-band insertion loss characteristics were compatible with a common bandpass filter configuration realizable in microstrip. The filtering requirements are shown in Table 5-5.

The transmitter filtering requirement was analyzed using an in-house computer program. The bandpass response shown in Figure 5-11 is indicative of the theoretical response expected from the 3-resonator edge-coupled filter utilized in the AESPA module. This particular configuration was computer optimized to achieve a more narrow bandpass and the gain/phase responses are shown in Figure 5-12. Fabrication and evaluation of this particular filter indicated an off-center bandpass (f_c=2252 MHz) and the resonator lengths were shortened from 0.990 inches to 0.970 inches; this configuration was then reoptimized using computer-aided design techniques. The theoretical results for this iteration are shown in Figure 5-13.

Filters from this design iteration were fabricated and evaluated on two different substrate thicknesses; 0.025 inch and 0.040 inch. Data obtained on the 0.040-inch substrate material is presented in Figure 5-14. Curves 1 and 2 represent typical initial filter characteristics obtained in two separate units fabricated from the same mask. These responses are typically centered low in frequency (approximately 2170 MHz). Curve 3 represents the filter response of Unit No. 1 after laser trimming the metallization 0.010 inches at each end of all coupled lines. Curve 4 represents the filter response of Unit No. 3 after laser trimming the metallization 0.020 inches at each end of all coupled lines. The observed frequency shifts were linear with respect to the amount of metallization trimmed and were on the order of +4 MHz per 1.0 mil of trim. Typical rejection data is also noted near the bottom of Figure 5-14.

Data obatined on the 0.025-inch substrate material is presented in Figure 5-15. Curves 1 and 2 represent typical initial filter characteristics obtained on two separate units fabricated from the same mask. These responses are typically centered high in frequency (approximately 2262 MHz). Curve 3 represents the filter response of Unit No. 5 after adding gold-ribbon "trim" tabs to extend resonator lengths approximately 0.005 - 0.010 inches. This centered the filter response about the transmit bandpass and typical rejection characteristics are noted on Figure 5-15.

In-band insertion loss of both filters is shown on the expanded scale of Figure 5-16. Higher losses associated with the use of 0.025-inch alumina are attributed mainly to the lower Q's associated with the thinner microstrip resonators.



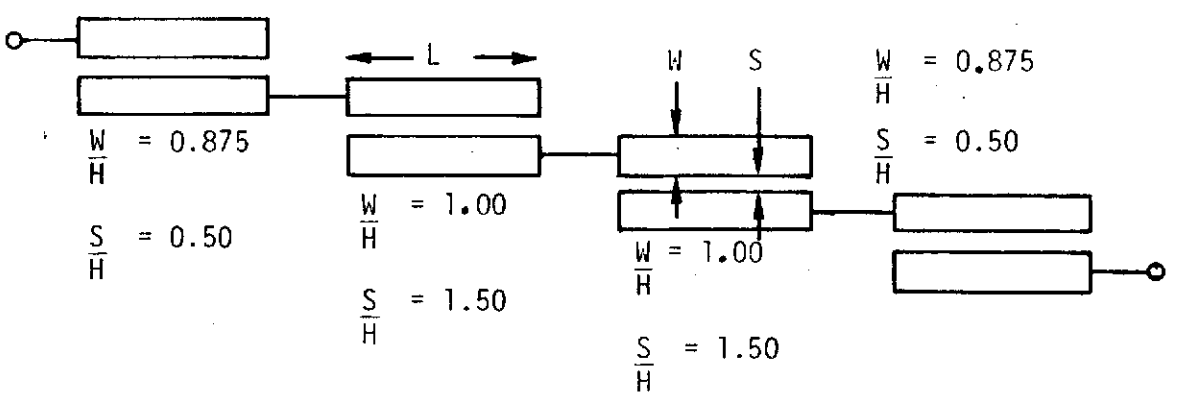


Figure 5-11. Theoretical Performance, AESPA IV Transmit Filter

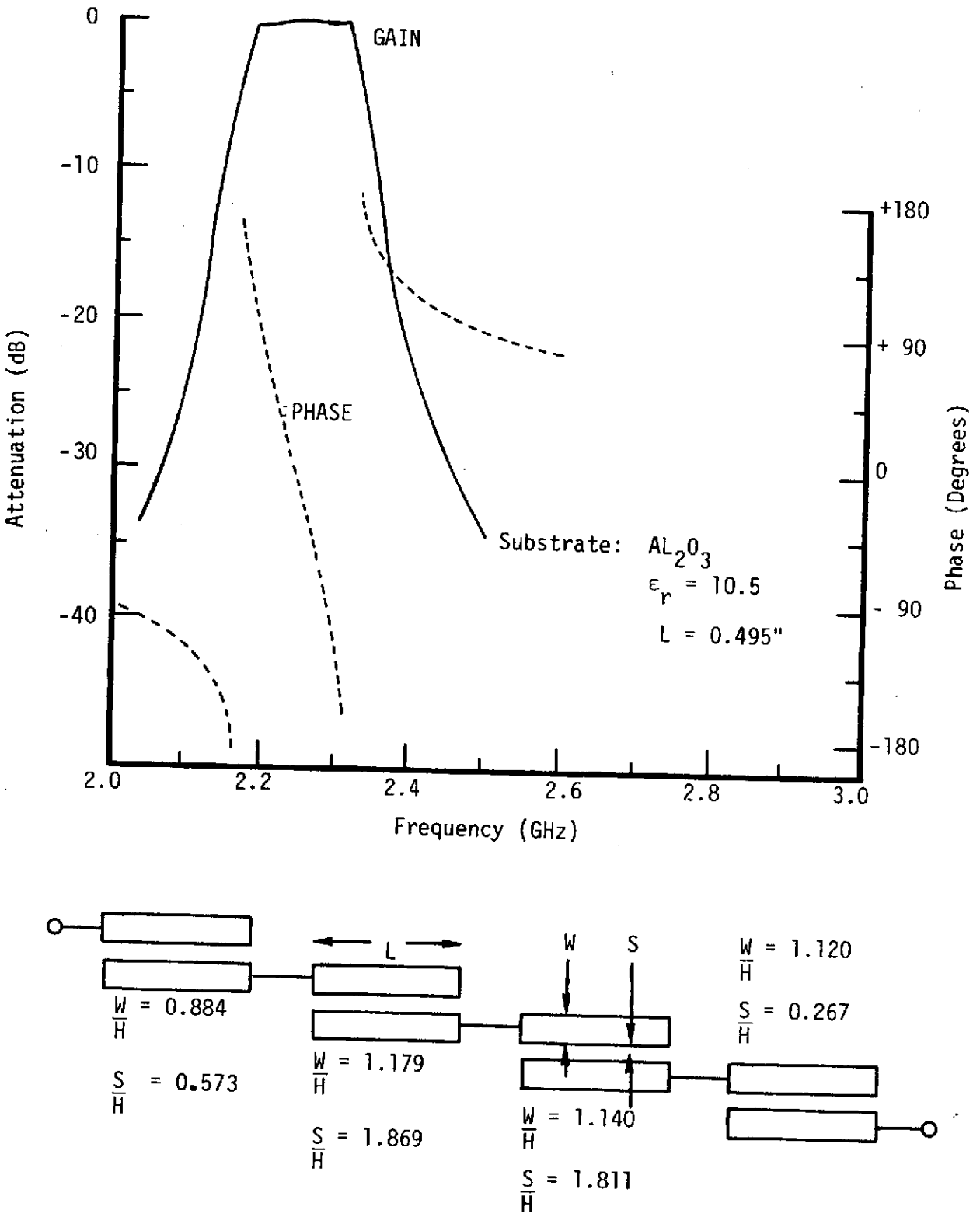


Figure 5-12. Theoretical Performance, SPACS I Transmit Filter

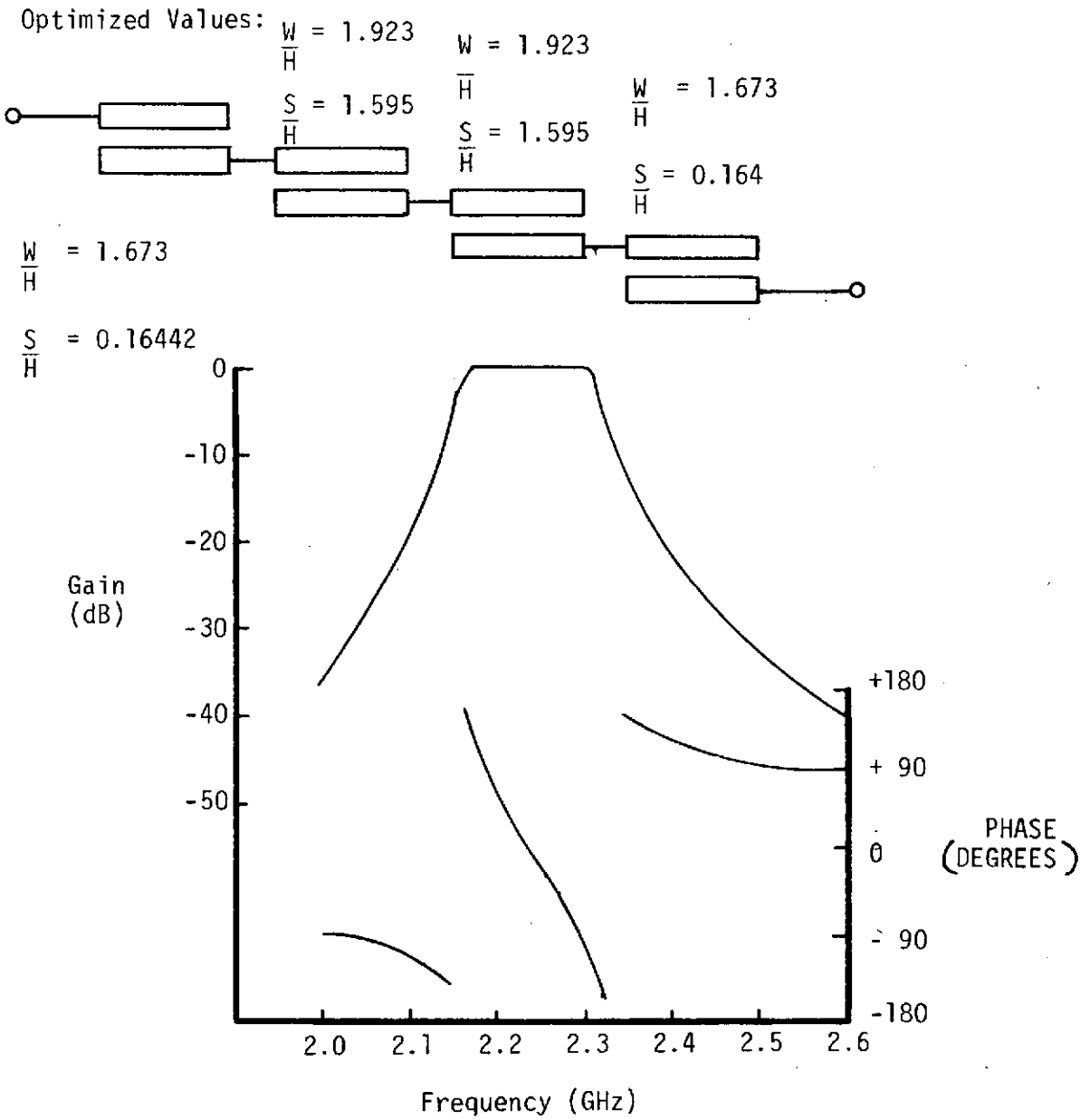


Figure 5-13. Theoretical Results, SPACS I Trnasmitter Bandpass Filter, Second Iteration

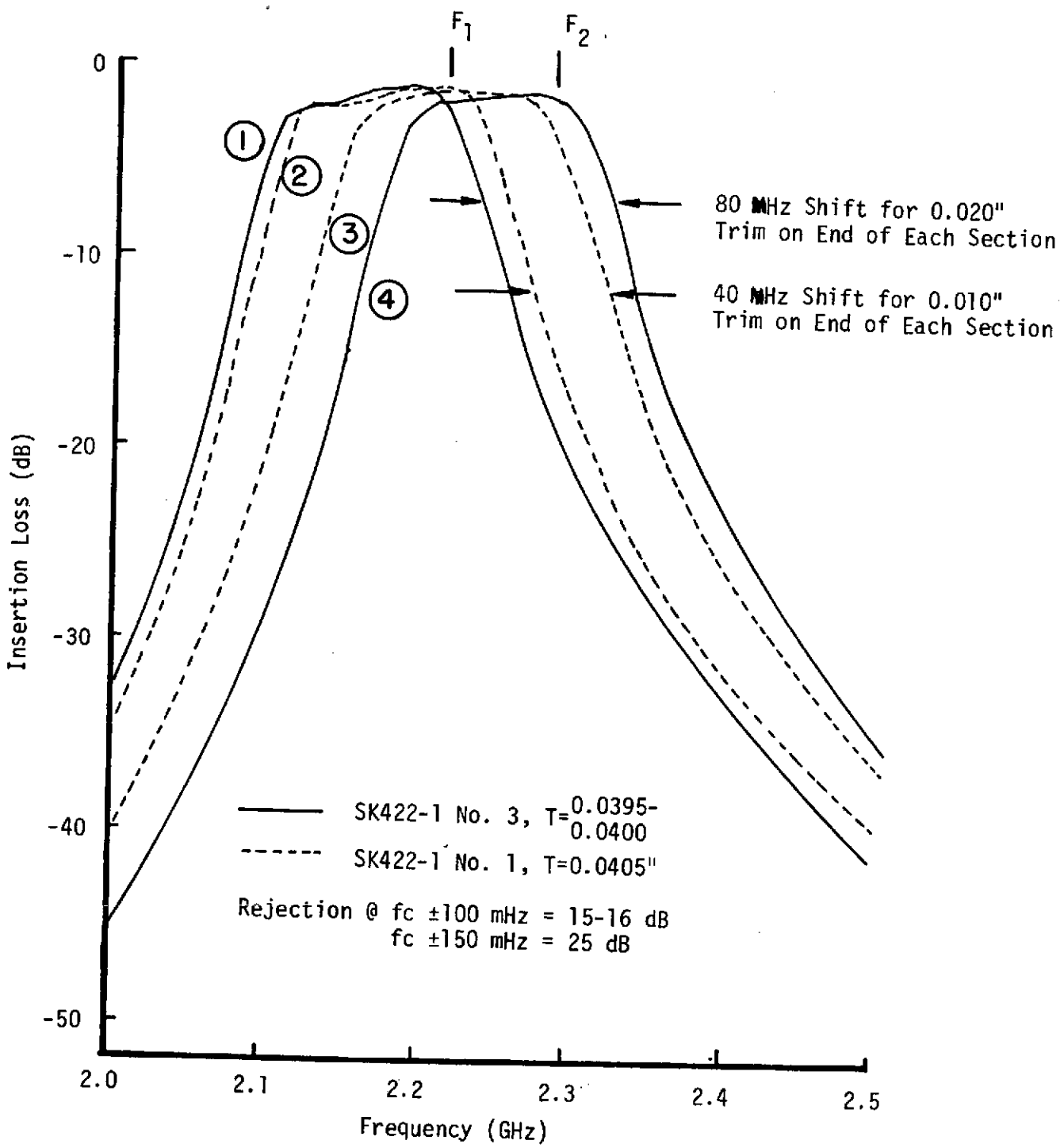


Figure 5-14. SPACS I Transmit Filter, 0.040 Inch Thick Alumina

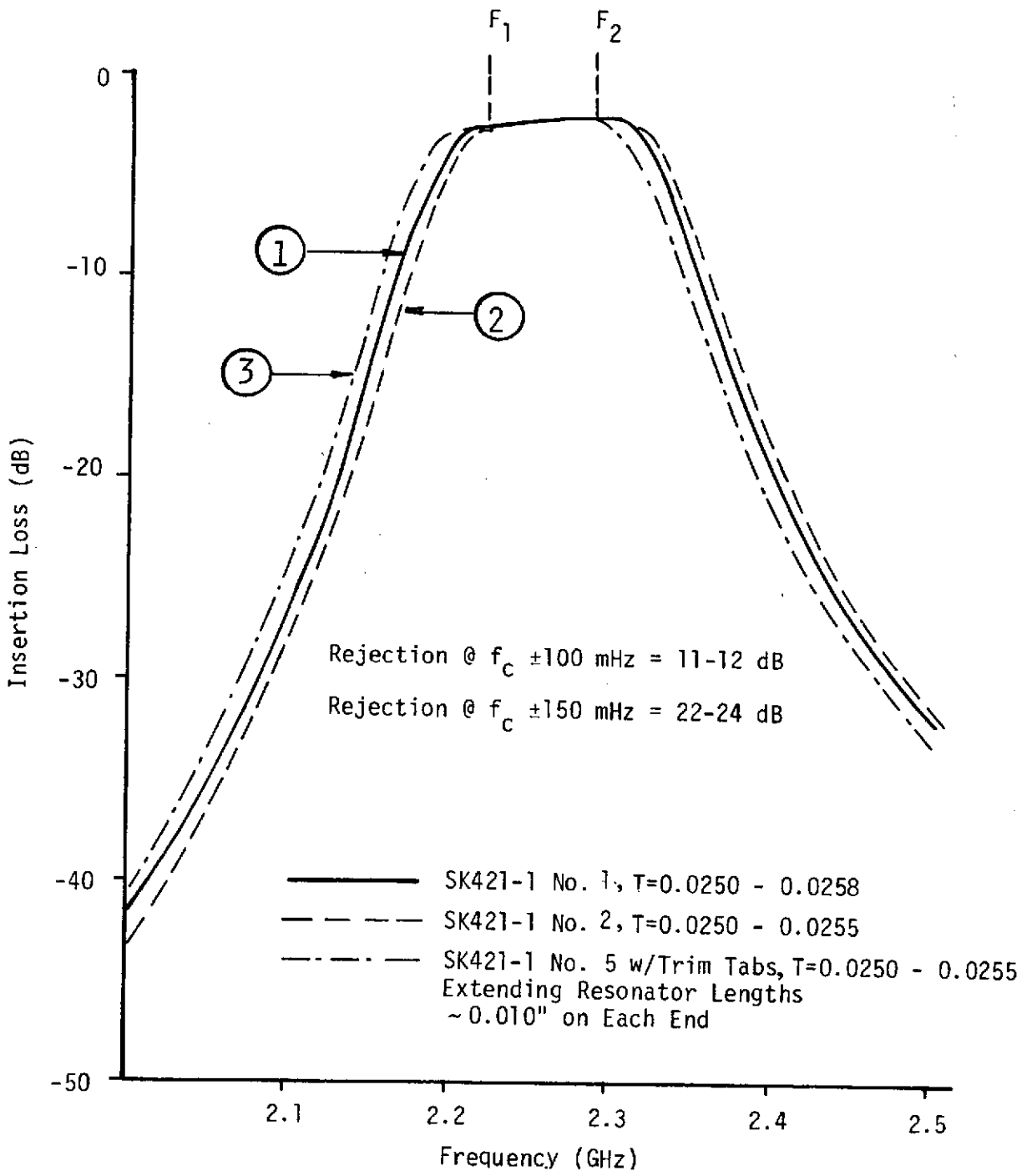


Figure 5-15. SPACS I Transmit Filter, 0.025 Inch Thick Alumina

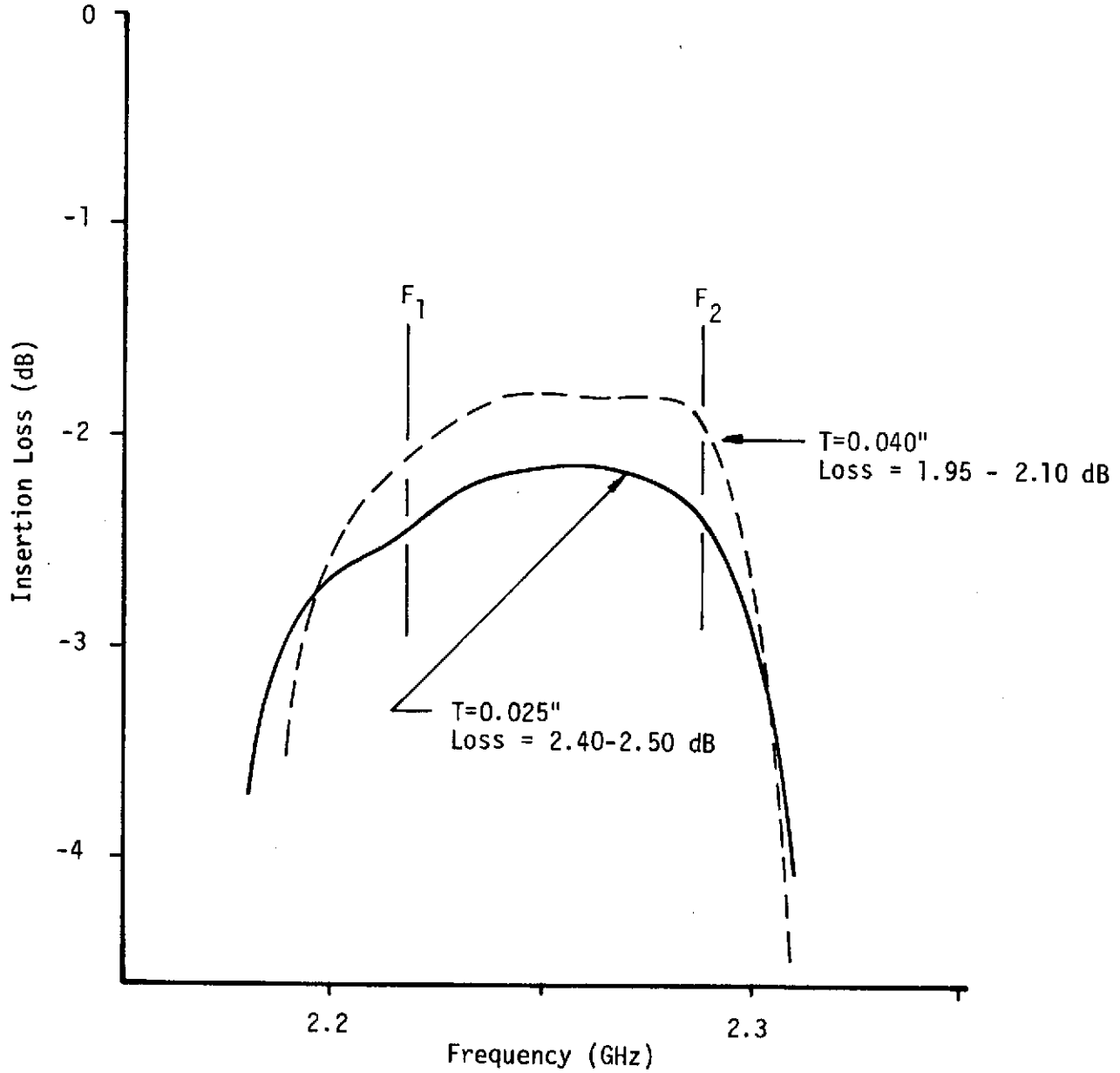


Figure 5-16. SPACS I Transmit Filter, Passband Insertion Loss

A decision was made to incorporate the lower loss 0.040 inch design into the final module design. Passband insertion loss was typically 0.4 dB lower than the 0.025-inch filter and the obtained rejection characteristics were slightly better. Resonator lengths were modified on the new mask to minimize trimming. Modification of the resonator lengths at the mask generation level resulted in a filter configuration which met the requirements without the need for any physical circuit "trimming." Actual data measured on the Automatic Network Analyzer (ANA) is shown in Figures 5-17 and 5-18. Passband insertion loss data is presented in Figure 5-17 for nine fabricated networks. Loss at the actual transmit frequencies varied from a minimum of 1.30 dB to a maximum of 2.35 dB. When compared to the module requirement of 2.0 dB maximum insertion loss at the transmit frequencies, it is noted that:

- Two (2) of the filters are exceptional (22% of the sample group)
- Three (3) other filters exceed the requirement by a substantial margin (33% of the sample group)
- Two (2) other filters meet the requirements (22% of the sample group)
- Two (2) other filters do not meet the requirement, but could be easily trimmed to be acceptable though marginal units (22% of the sample group).

These results represent a working yield of 78% on the edge-coupled microstrip filter with no tuning or trimming required. The narrow-band characteristic (5.3%, 3 dB bandwidth) of the transmit filter is shown in Figure 5-18. A comparison of the transmit filtering requirements and achieved results is shown in Table 5-5.

4. Receive Filter Design

The receiver bandpass filtering requirement (Table 5-6) was originally identified as a critical item in the development of a viable module design. Operation of the module in the fully duplexed mode with a low noise receiver front-end, a high-gain (33 dB) receiver RF amplifier, a relatively high-level transmitter (+35 dBm at antenna), and the necessary size/weight constraints required a state-of-the-art solution to the filtering problem. Three filter configurations were considered and evaluated in reaching the final module filter.

One such approach was the interdigitated stripline approach shown in Figure 5-19. This particular design was available in-house as a result of filtering requirements on another program. This filter was a 9-element (7 resonators/2coupling sections) interdigitated filter built on two layers of bonded Duroid material (ε_r = 2.2) with a total thickness of 0.125 inches. Insertion loss as a function of frequency for this filter is shown in Figure 5-20. Although transmit bandpass rejection was more than adequate (in excess of 60 dB), receive bandpass insertion loss was not compatible with the receiver noise figure requirement and this approach was abandoned.

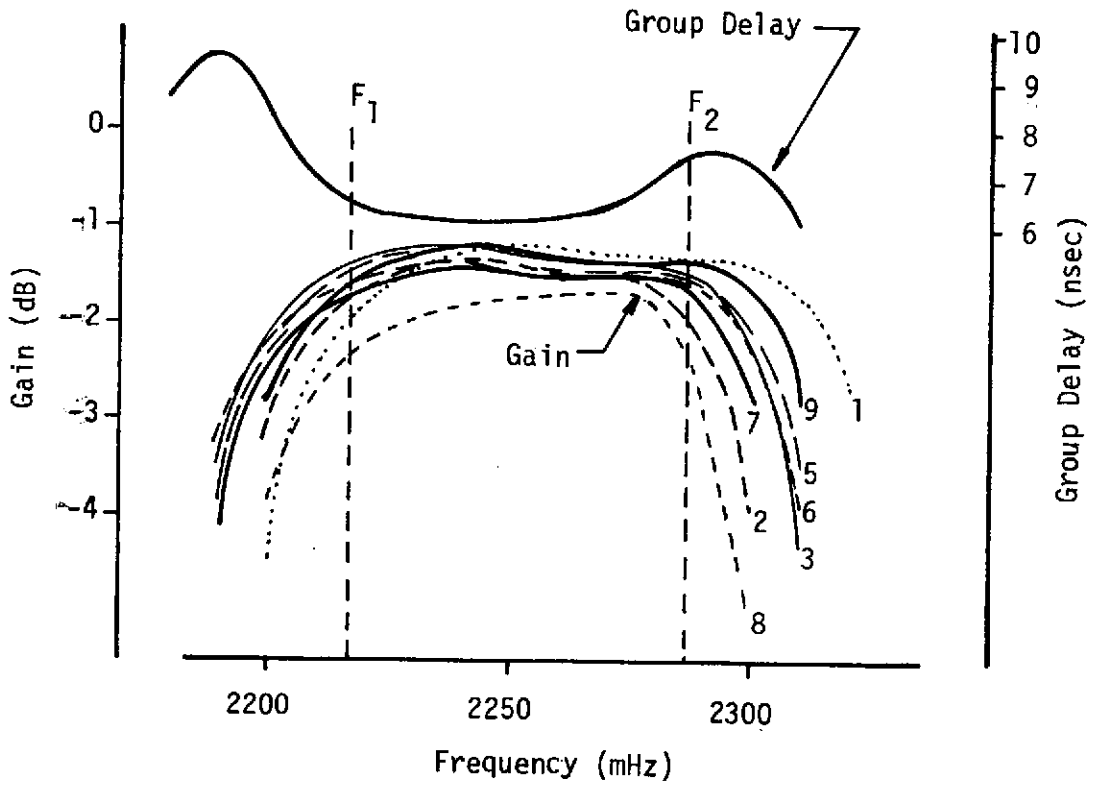
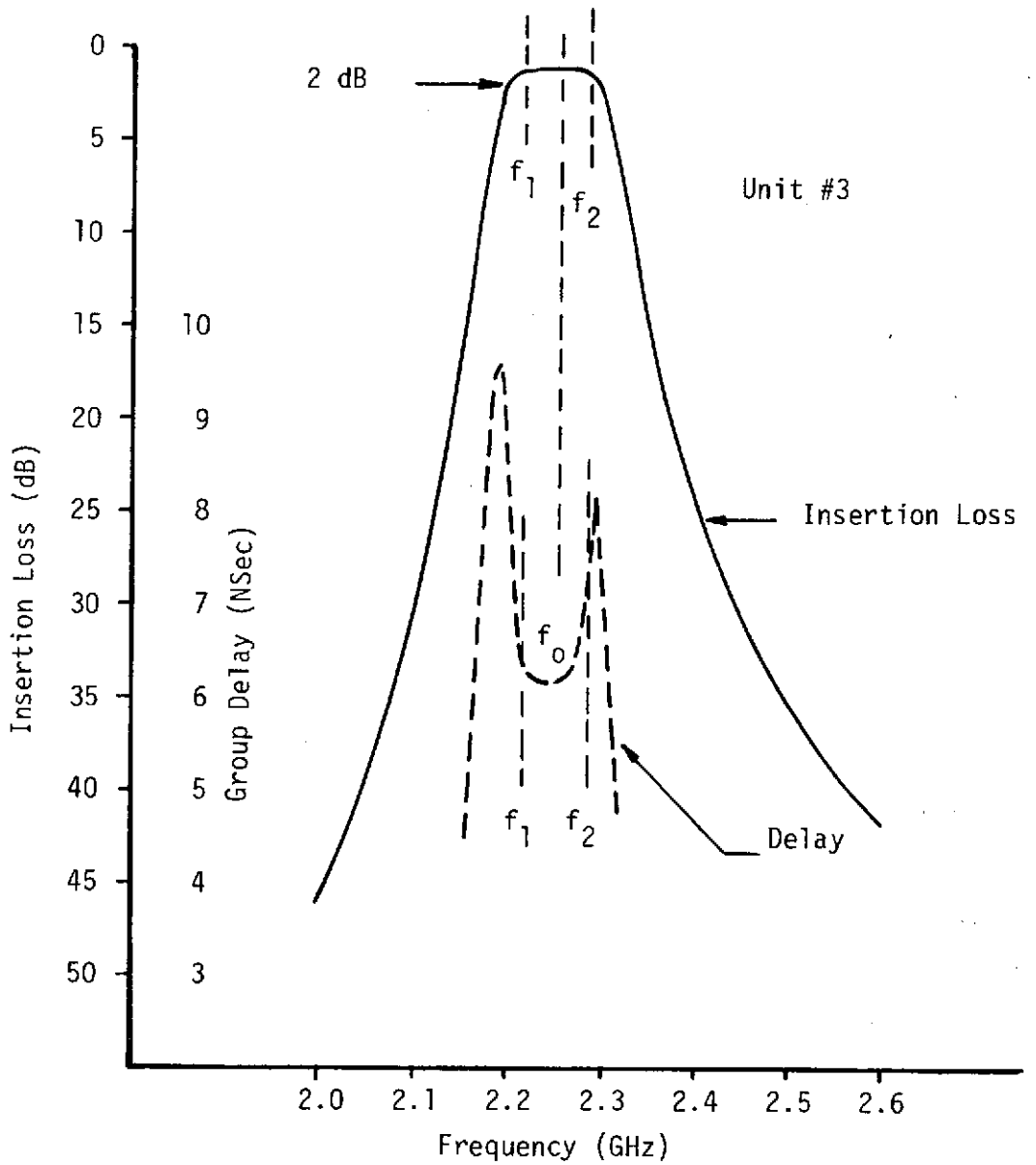


Figure 5-17. Passband Insertion Loss, Final Configuration, SPACS I Transmit Filter



Loss @ $f_o \pm 100$ mHz ≥ 15 dB

Loss @ $f_o \pm 150$ mHz ≥ 25 dB

Figure 5-18. Rejection Characteristic, Final Configuration, SPACS I Transmit Filter

TABLE 5-5. SPACS I MODULE TRANSMIT FILTER

PARAMETER	REQUIREMENT	RESULT
Center Frequency	2252 MHz, Typ.	2252 MHz
0.5 dB Bandwidth	7%, Typ.	4%, Typ.
Midband Loss	2 dB, max.	1.4 dB, Typ.
		1.8 dB, Max.
Rejection at $f_c \pm 100$ MHz	10 dB, min.	15 dB
Rejection at $f_c \pm 150$ MHz	20 dB, min.	25 dB

TABLE 5-6. SPACS I MODULE RECEIVE FILTER

PARAMETER	REQUIREMENT	RESULTS
Center Frequency	2074 MHz, Typ.	2072 MHz, Typ.
1-dB Bandwidth	110 MHz, min.	120 MHz, Typ.
Insertion Loss		
@ 2030 MHz	1.0 dB, Typ.	1.0 dB, min.
	1.7 dB, Max.	1.9 dB, max.
@ 2118 MHz	1.0 dB, Typ.	0.9 dB, min.
	1.7 dB, Max.	2.1 dB, max.
@ 2215 MHz	45 dB, min.	45.8 dB, min.
		46.3 dB, max.
Input VSWR (within 1-dB Bandwidth)	2.5:1, max.	2.2:1, max.
Temperature Stability		

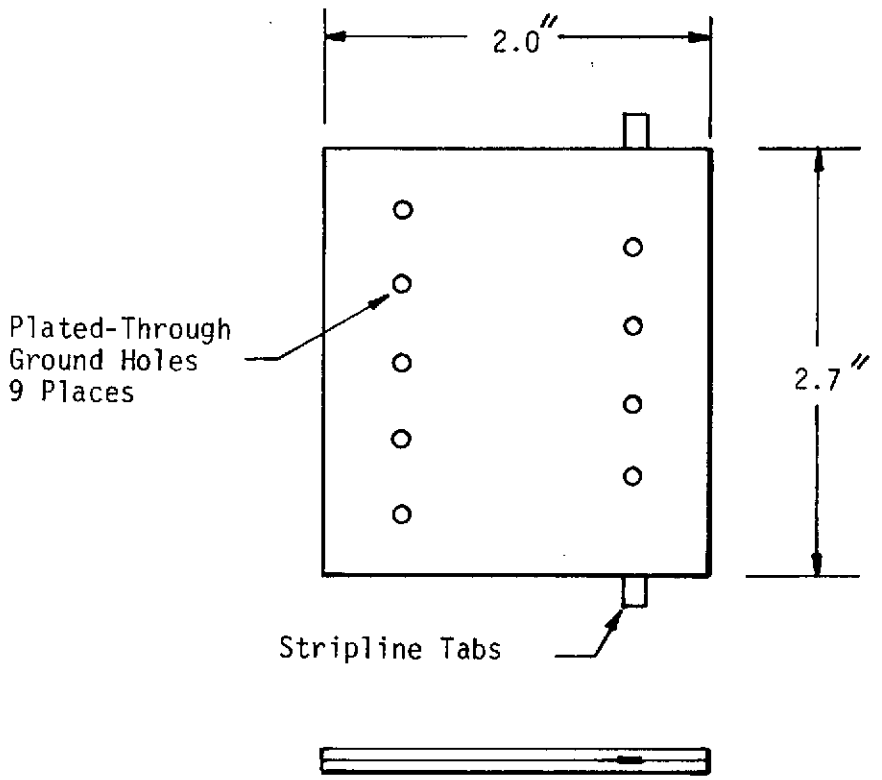


Figure 5-19. Outline Drawing, 7-Element Interdigital Stripline Filter

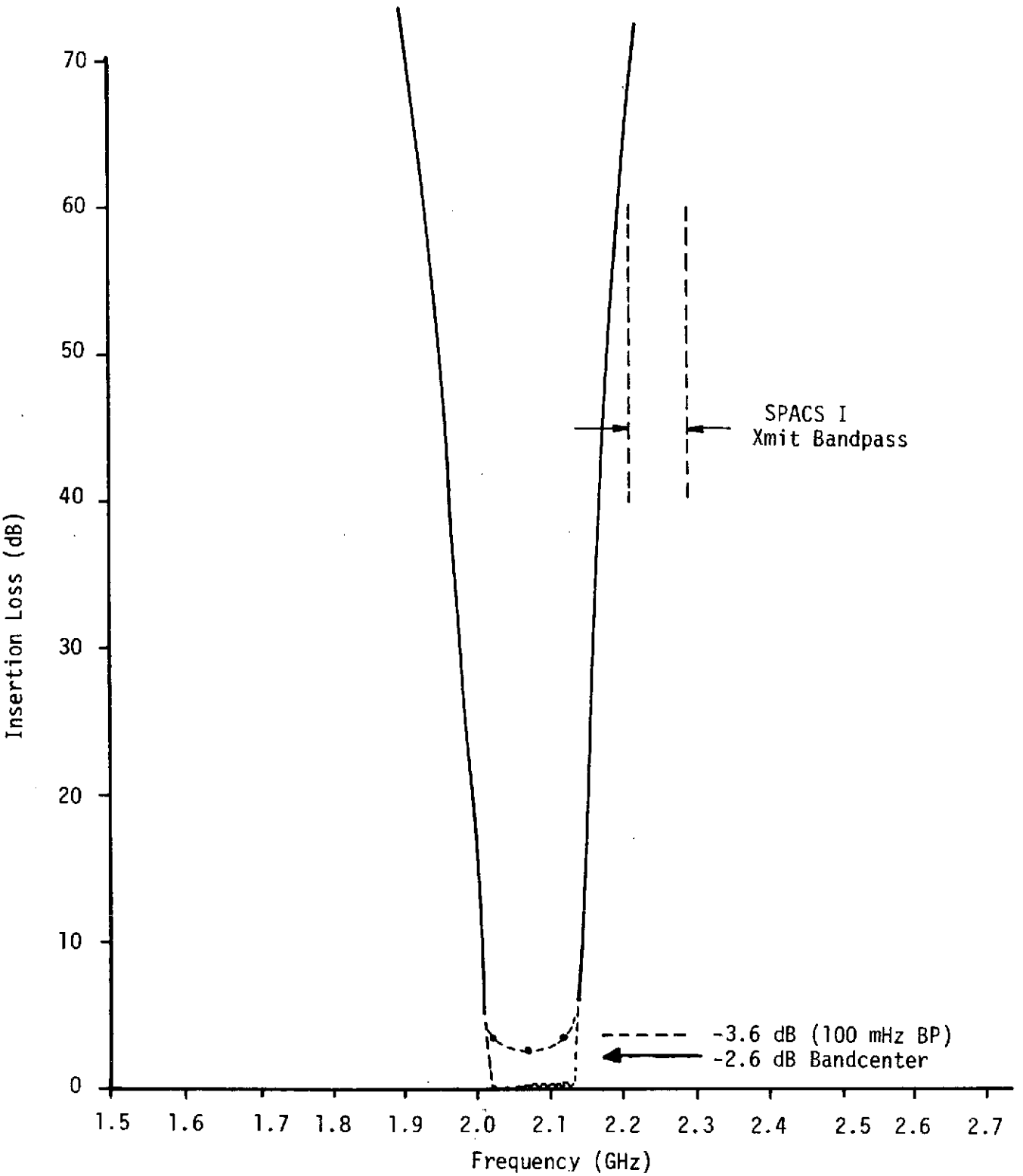


Figure 5-20. Insertion Loss As A Function of Frequency, 7-Element Interdigital Stripline Filter

A second approach was to design and evaluate a "suspended-substrate" filter in a closed cavity. The basic design was specified as follows:

- Chebyshev response
- 0.2 dB amplitude ripple
- 2.022-2.126 GHz equiripple bandwidth
- 45 dB attenuation at 2.210 GHz
- Ground plan spacing of 0.100 inch
- $\varepsilon_r = 1.0$
- $Z_o = 50$ ohms

This configuration was basically stripline in air and was achieved by etching the 7-element (5-resonator) interdigitated pattern on 0.005-inch thick kapton; the kapton material was suspended within a 0.100-inch cavity.

The best performance achieved with this configuration is shown in Table 5-7 and insertion loss is graphed for comparison with the theoretical performance in Figure 5-21. In-band insertion loss could not be reduced to less than 3 dB; this was incompatible with noise figure requirements and a decision was made to purchase a comb-line filter from Sonoma Engineering.

A comb-line filter prototype unit, centered slightly high in frequency, was obtained for evaluation testing. This filter was evaluated over a temperature range of 14 - 68 degrees centigrade and performance is shown in Figure 5-22. Overall filter performance was found to be compatible with SPACS requirements and a procurement specification was released.

The broadband rejection and passband insertion loss characteristics are shown graphically in Figures 5-23 and 5-24 for the two prototype units delivered during the course of the contract. The configuration is also depicted schematically in Figure 5-25. Performance results of these filters are also compared to the requirements listed in Table 5-6.

5. Transmit Isolator and Module Duplexer Design

Miniature "drop-in" circulators were required to perform the duplexing function at the module antenna port and to isolate transmitter power amplifier from antenna mismatch conditions. These units were specified for operation over the unique frequency bands associated with the SPACS I system and requirements are given for the duplexer in Table 5-8; requirements for the transmit isolator are given in Table 5-9.

The particular units used in the SPACS I breadboard module were procurred from TRAK Microwave Corp., Tampa, Florida. Performance results are compared with the requirements in Tables 5-8 and 5-9. The physical

TABLE 5-7. SUSPENDED-SUBSTRATE
RECEIVE FILTER PERFORMANCE

FREQUENCY (MHz)	VSWR (RATIO)	GAIN (dB)	GROUP DELAY (NSECS)
1980	1.77	-4.55	9.23
2000	1.54	-3.87	9.21
2020	1.17	-3.05	8.32
2040	1.15	-2.84	8.27
2060	1.19	-3.04	8.55
2080	1.37	-3.09	9.43
2100	1.50	-4.06	13.08
2120	4.86	-9.60	9.31
-			
2210	19.8	-46.5	-
2290	17.9	-65.1	-

TABLE 5-8. DUPLEXER (CIRCULATOR), SPACS I MODULE

PARAMETER	REQUIREMENTS	RESULTS
Center Frequency	2165 MHz	2165 MHz
Bandwidth	12.5% (2030-2300 MHz)	12.5%
Isolation	18 dB, min.	22 dB, min.
Insertion Loss	0.6 dB, max.	0.7 dB, max.
VSWR	1.30:1, max.	1.4:1, max.

T_1 = LOWER TRANSMIT FREQUENCY (2217.5 MHz)

R_1 = LOWER RECEIVE FREQUENCY (2041.9 MHz)

R_2 = UPPER RECEIVE FREQUENCY (2106.4 MHz)

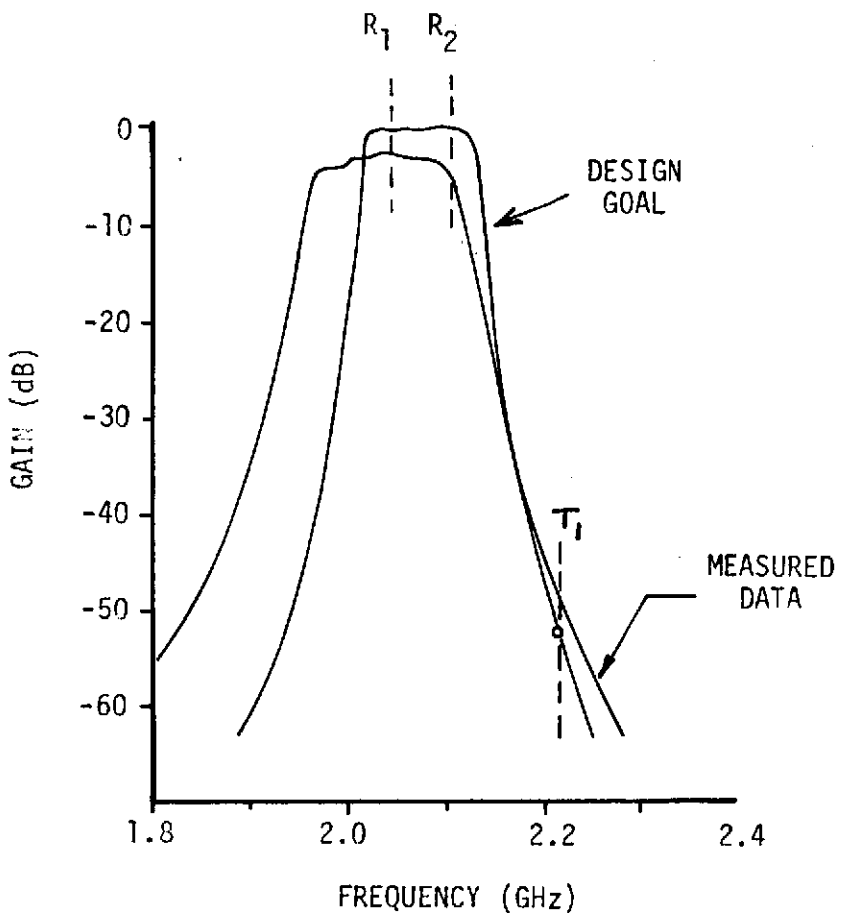


Figure 5-21. Performance Comparison, Suspended-Substrate Receiver Filter and Design Goal

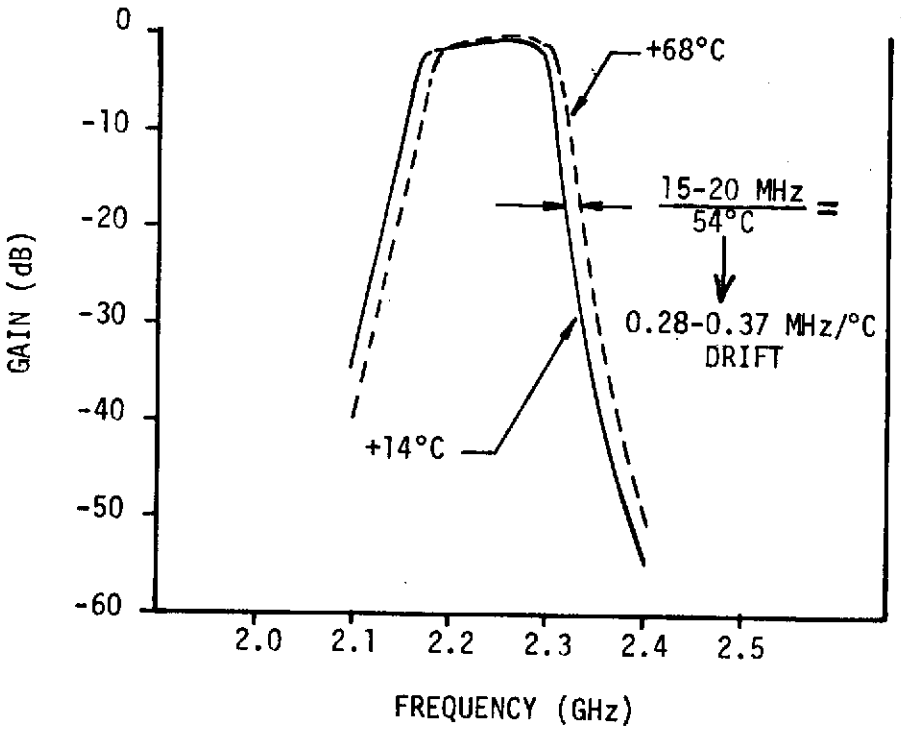


Figure 5-22. Temperature Evaluation, Sonoma Comb-Line Filter

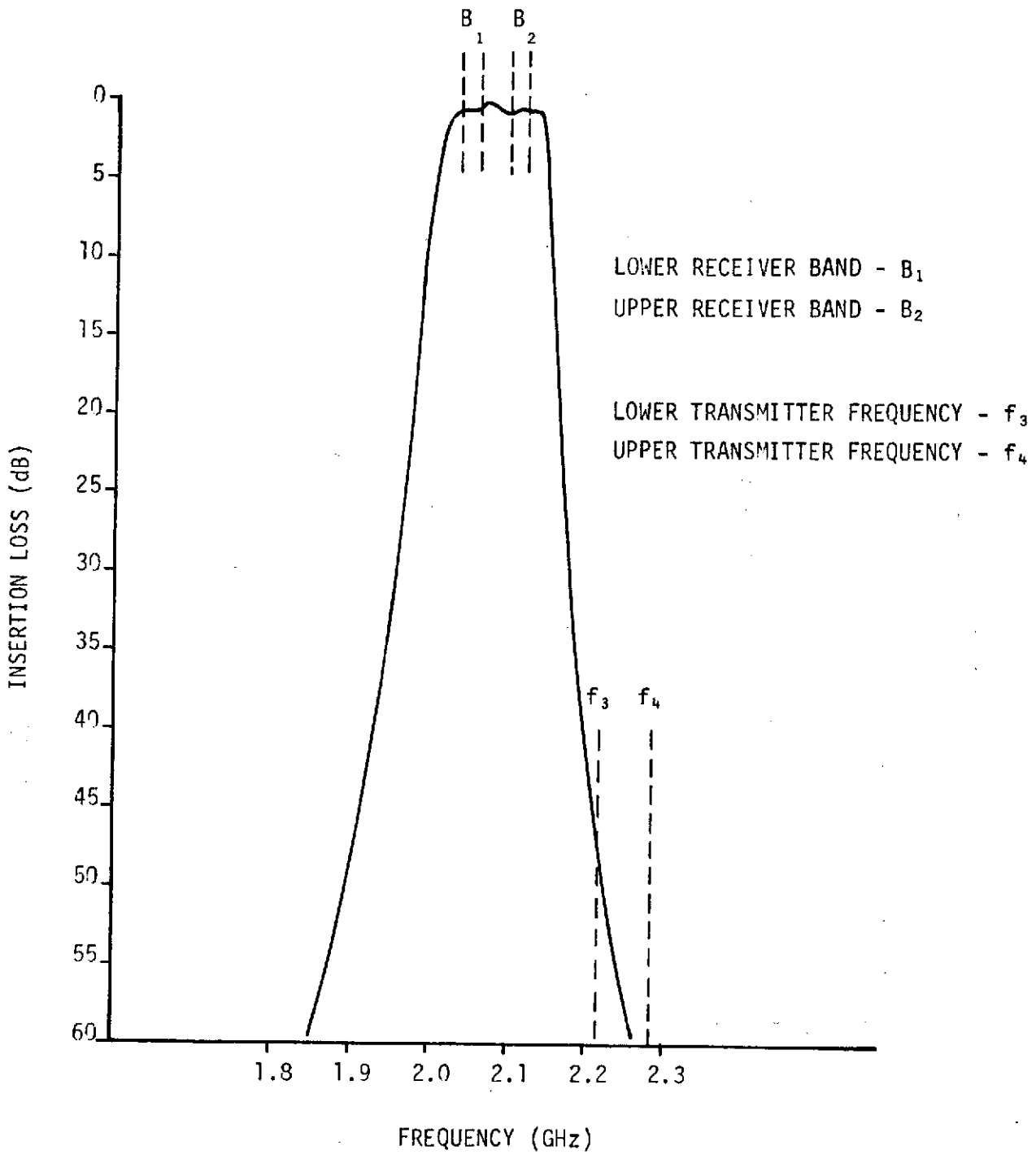


Figure 5-23. Rejection/Passband Characteristics, SPACS I Receive Filter

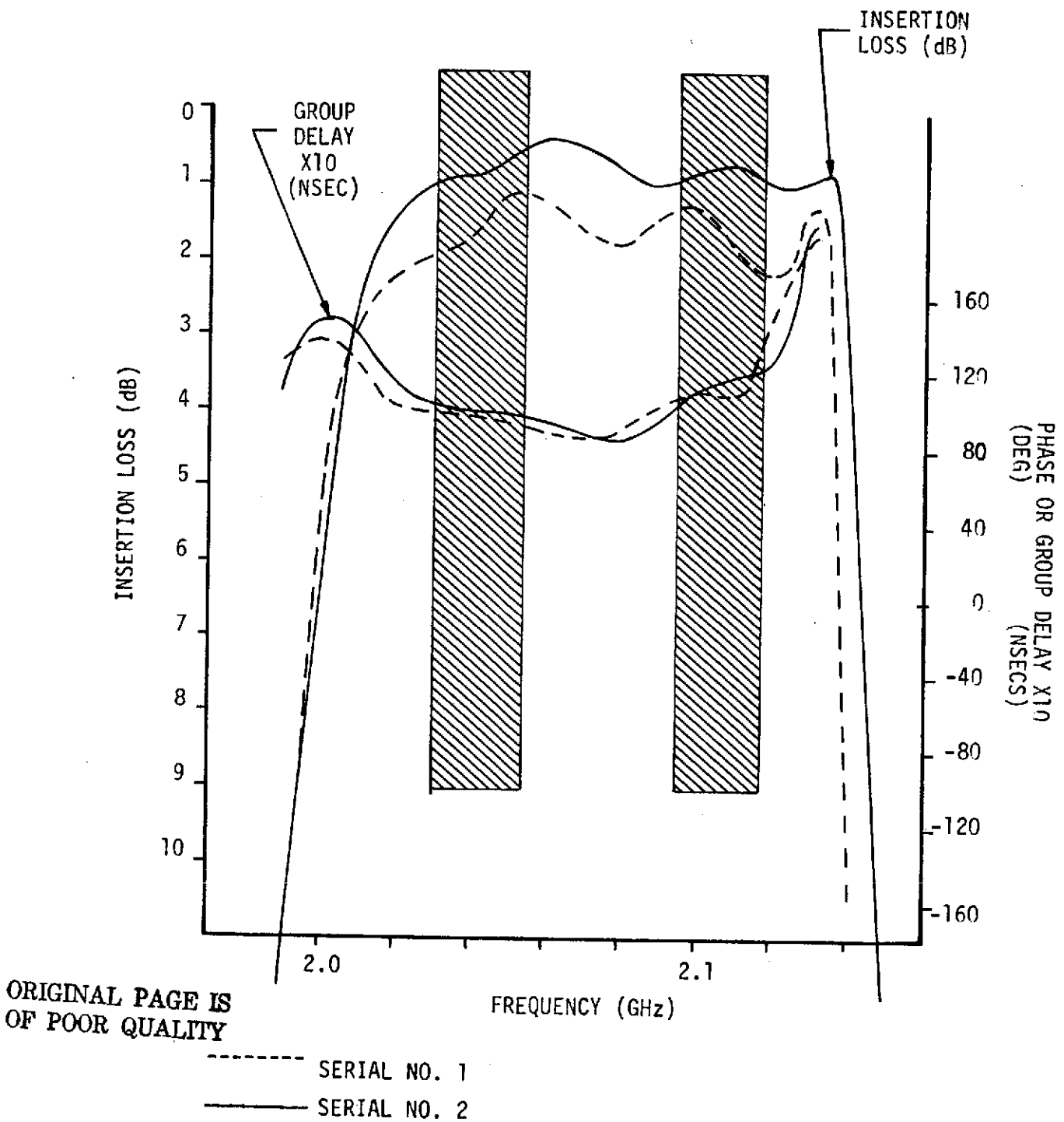


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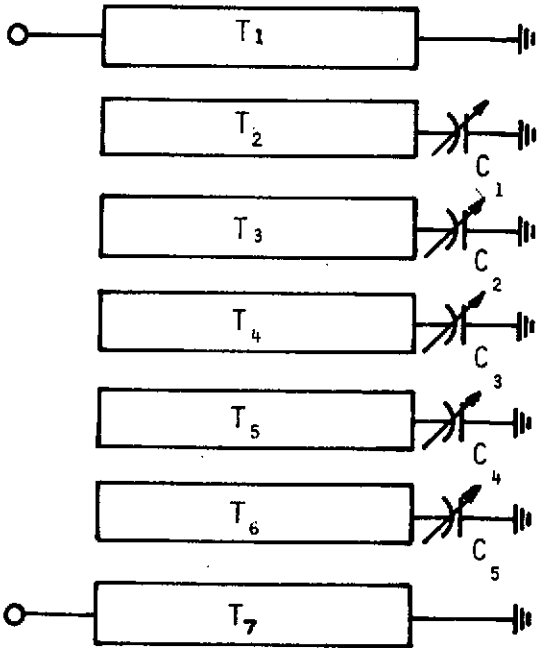
Figure 5-24. Passband Insertion Loss, SPACS I Receive Filter



T_1, T_7: Coupling Elements

T_2, T_6: Resonator Elements

C_1, C_5: Variable Capacitors (Establish Resonating Frequency)

Figure 5-25. Schematic, Receiver Combline Filter

size of each unit is 0.75 x 0.75 x 0.25 inches and the isolator is provided with a third-port termination in which to dissipate reflected energy which might attempt to re-enter the transmit channel.

6. Low Noise Amplifier Design

Module receiver electronic gain and noise figure requirements were satisfied through the design and development of a 3-stage low noise amplifier shown schematically in Figure 5-26. The amplifier utilizes the Avantek AT-4641 microwave transistor in each stage, with the bias currents optimized for minimum noise contribution and maximum output gain compression in the first and third stages, respectively.

Design procedure was based on the use of "black box" scattering parameters measured on the Avantek transistors. S-parameters were measured on several representative units over the frequency range 1900-2250 MHz for collector current levels of 5, 7, 10, 15, and 20 mA at a 10 volt V_{ce} level.

Noise figure measurements were also conducted on the AT4641 transistor as well as the Fairchild FMT-4005. A summary of these results is shown in Table 5-10; by virtue of its lower noise performance the AT4641 transistor was established as the prime device.

Gain compression measurements were conducted on the AT4641 and results are shown graphically in Figure 5-27. Since collector currents are limited to a maximum of 10 mA on the FMT-4005 transistor, it was not considered a contender for use in the higher level third stage.

Noise figure was minimized through the design of a network which transformed the driving point impedance of the comb-line filter, shown in Figure 5-28, to the optimum source impedance for minimum noise figure over each receive channel. Characterization of the optimum source impedance for minimum noise was accomplished in the test set shown in Figure 5-29. Adjustable screw tuners were used to minimize noise figure (input tuner) and to maximize gain (output tuner). The test set was then disassembled and source and load impedance measurements were made using the Hewlett-Packard Automatic Network Analyzer. The measured optimum source impedance is also shown on Figure 5-28. Computer-aided design techniques were utilized to optimize element values of the input network topology; the figure of merit used for this optimization was the mismatch loss between the transformed impedance of the comb-line filter and the required source impedance to minimize the noise figure of the AT-4641 transistor. This input network, with optimized element values, is shown schematically in Figure 5-30. The driving point impedance presented to the AT4641, with the input matching circuit terminated by the comb-line filter, is shown in Figure 5-31 along with the required optimum source impedance. The calculated mismatch loss between the transformed impedance and the required impedance is shown in Figure 5-32.

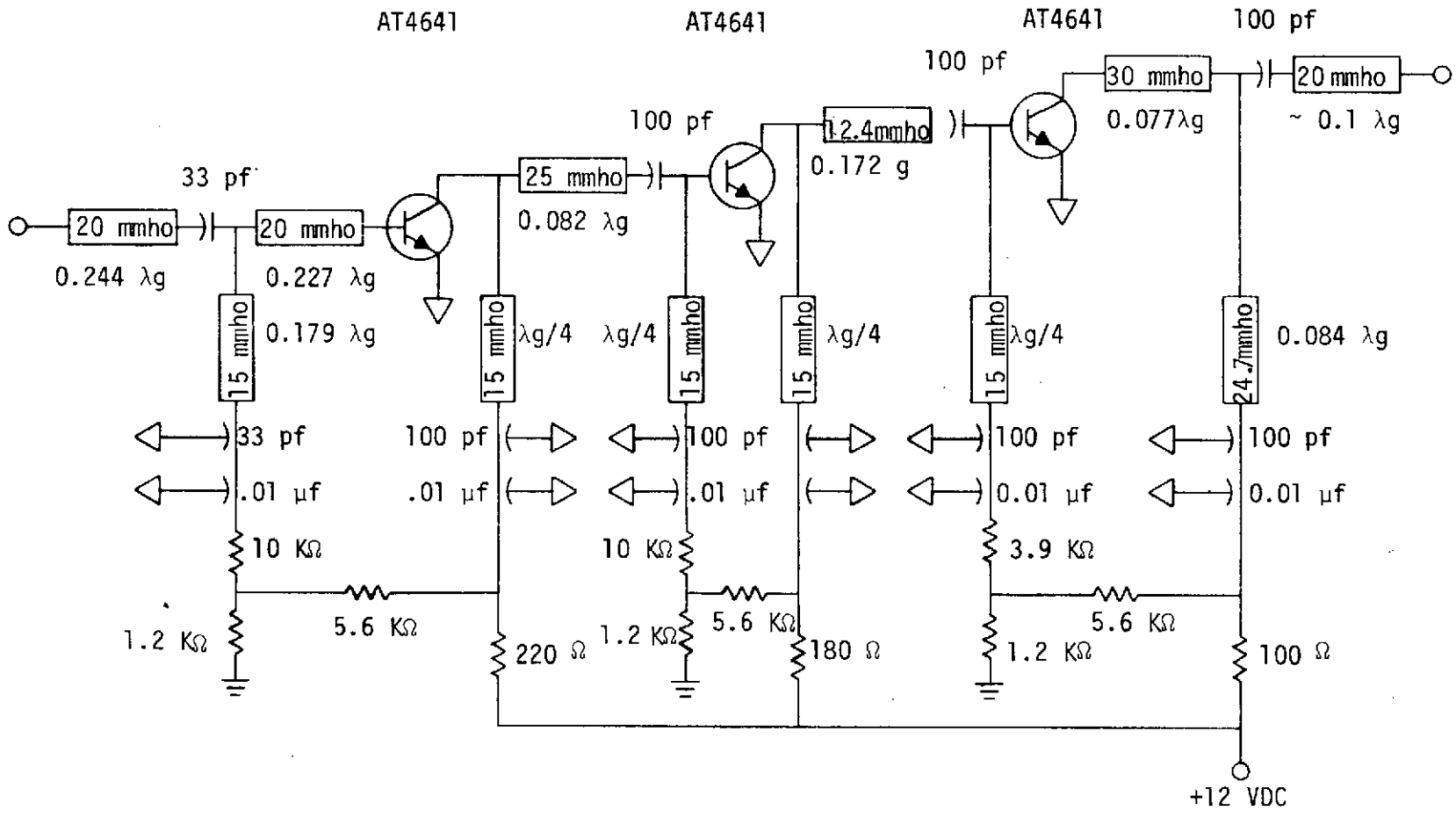


Figure 5-26. Low Noise Amplifier Configuration
SPACS I Module

TABLE 5-9. ISOLATOR, SPACS I MODULE

PARAMETER	REQUIREMENTS	RESULTS
Center Frequency	2252 MHz	2252 MHz
Bandwidth	5% (2196-2308 MHz)	5%
Isolation	20 dB, min.	22 dB, min.
Insertion Loss	0.5 dB, max.	0.4 dB, max.
VSWR	1.26:1, max.	1.4:1, max.

Table 5-10. Noise Figure Summary, SPACS I Low Noise Device Evaluation

Device	Unit No.	Gain (dB)	Noise Figure (dB)
FMT-4005	3	11.0	2.45
	4	10.0	2.61
	5	10.4	2.48
AT-4641	69	11.5	2.19
	73	10.5	2.31
	89	11.0	2.05

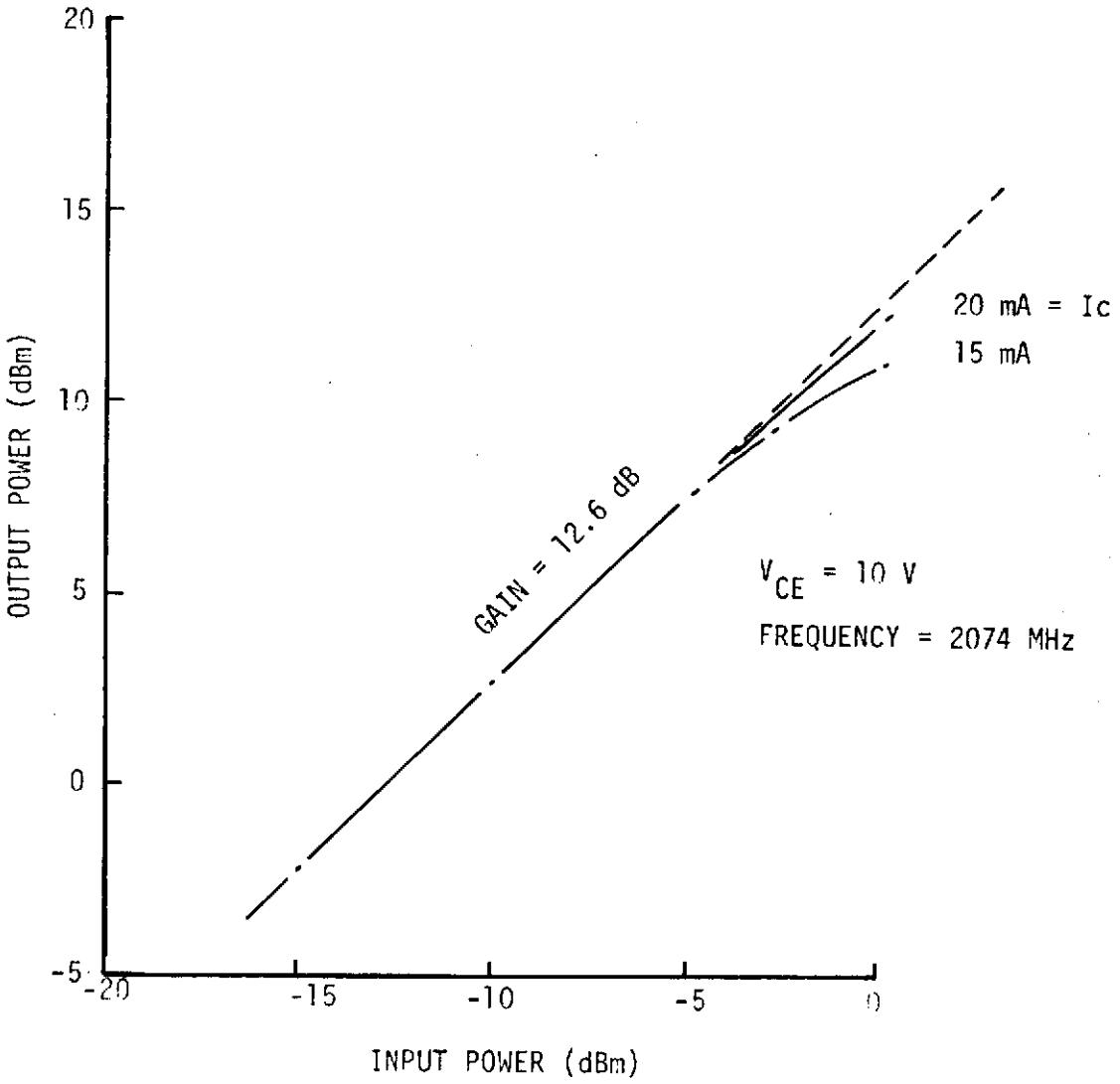


Figure 5-27. Gain Compression Characteristics, Avantek AT-4641 Transistor

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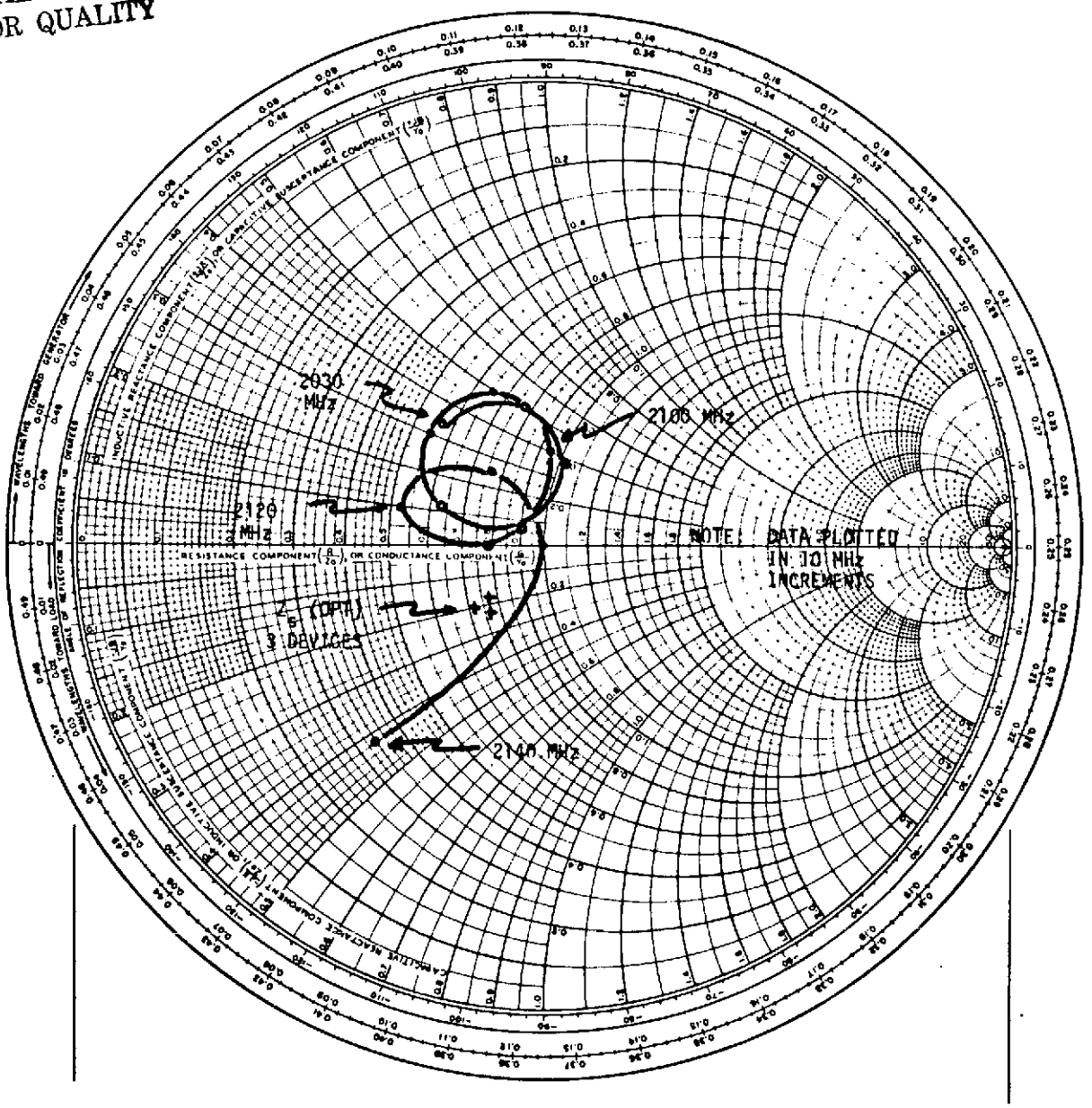


Figure 5-28. Driving Point Impedance, Comb-Line Filter, Low Noise Amplifier Port

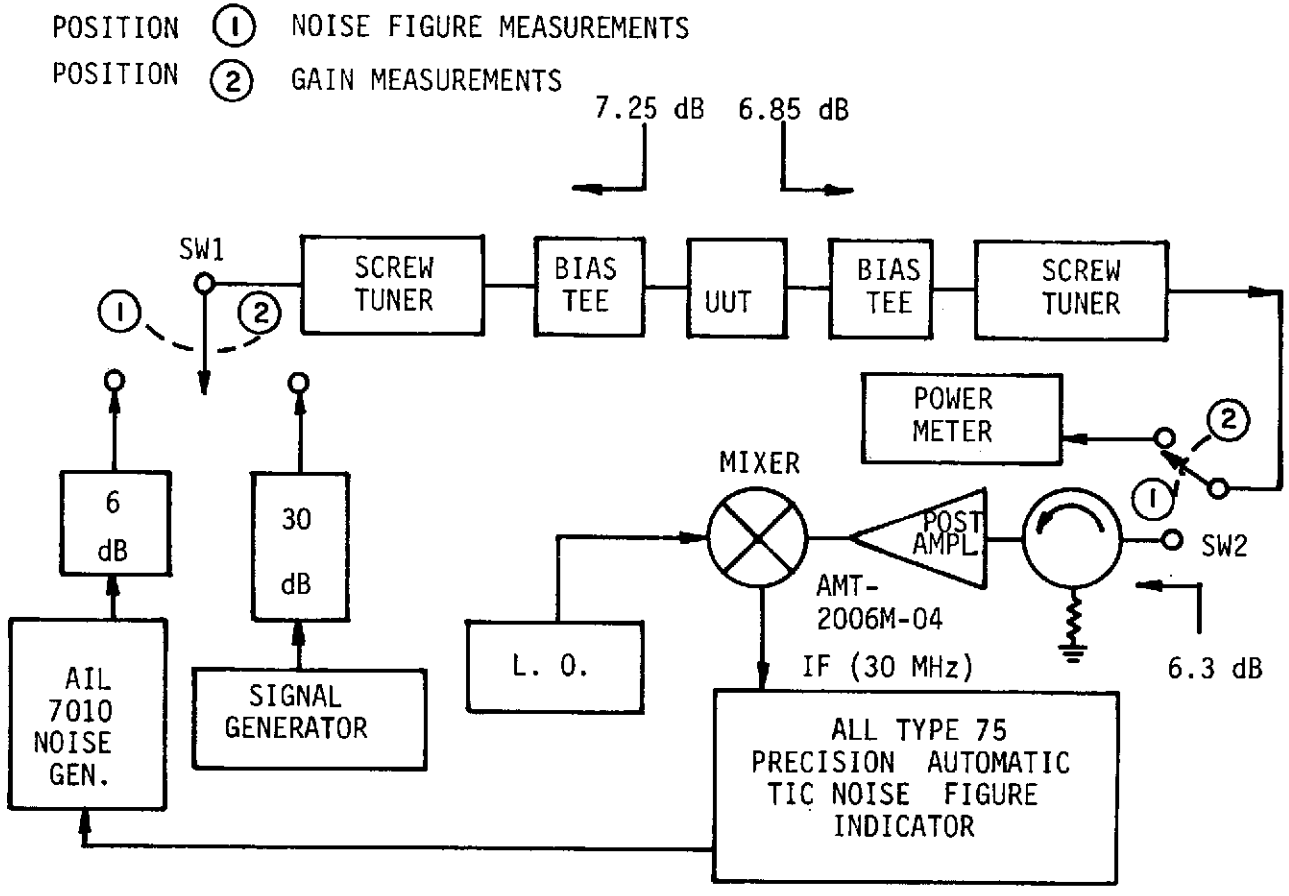
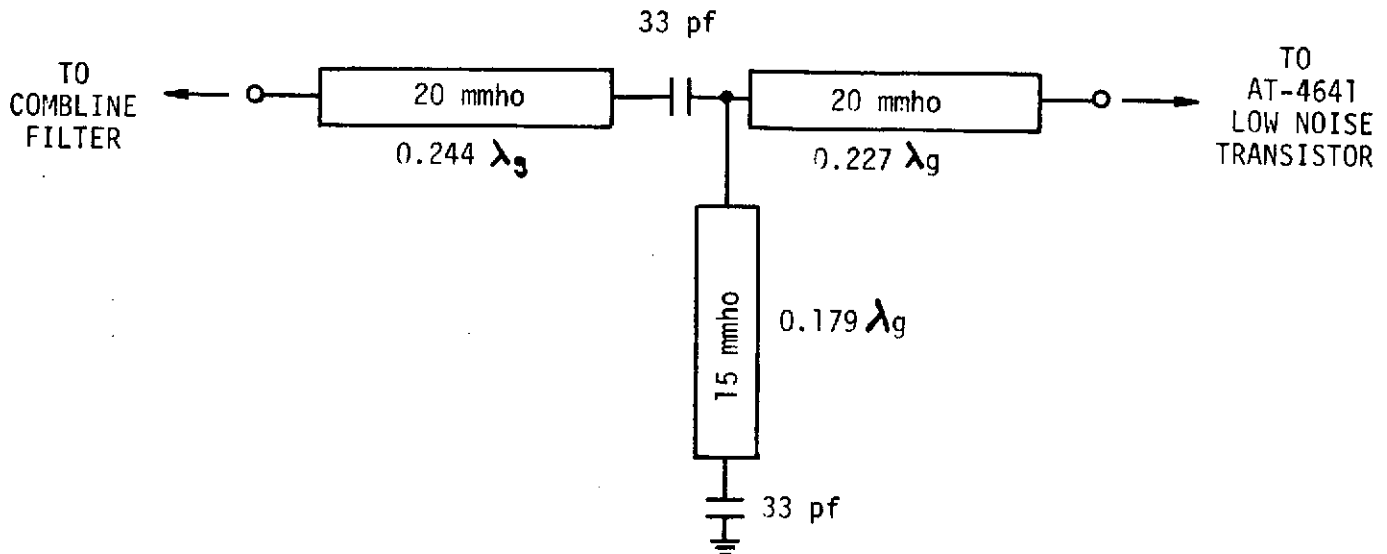


Figure 5-29. Noise Figure Test Set



NOTE: λ_g REFERENCED TO 2080 MHz

Figure 5-30. First Stage Noise Match, Low Noise Amplifier

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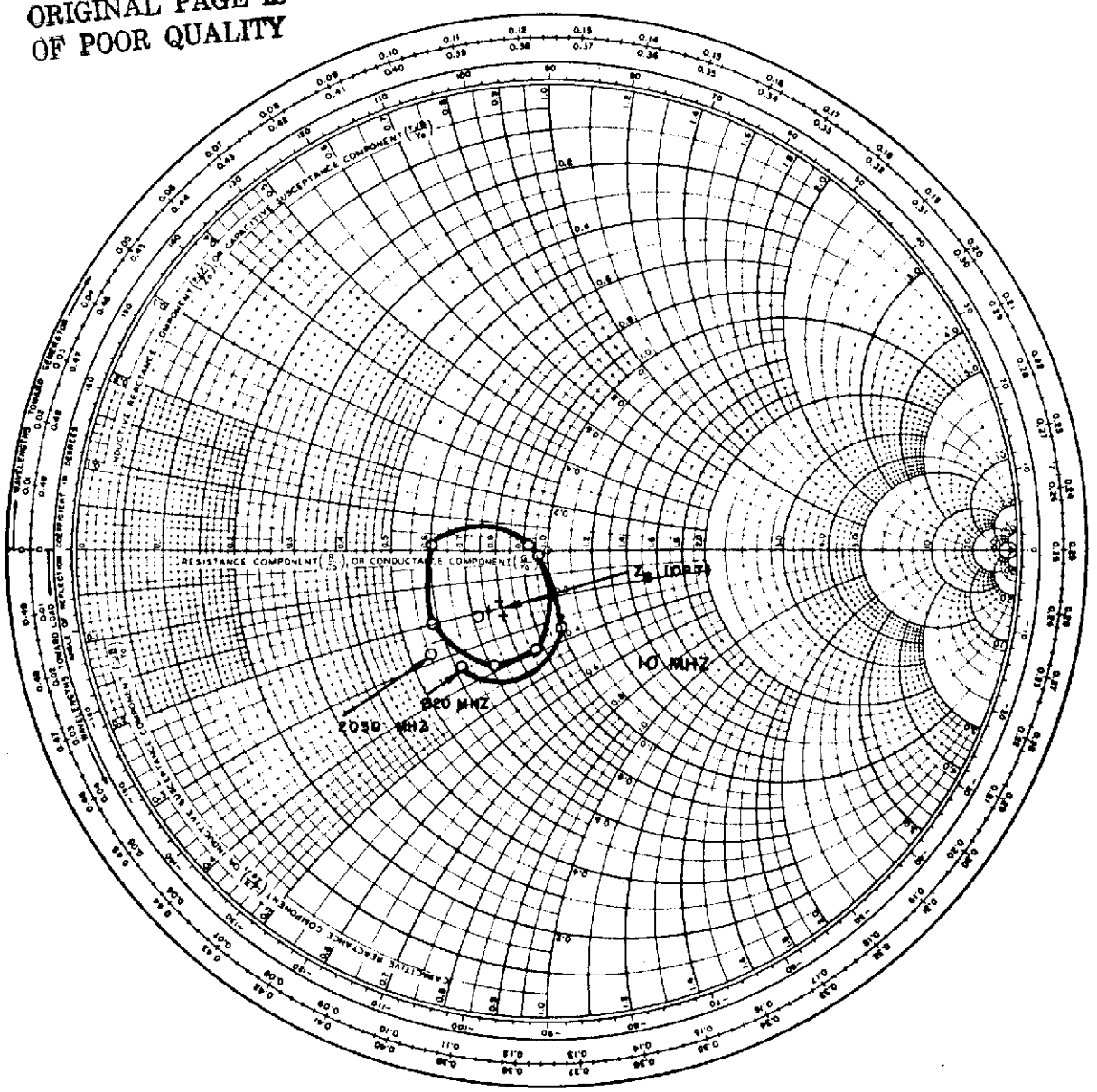

Figure 5-31. Source Impedance At Low Noise Device, Optimized Input Network Terminated Into Comb-Line Filter

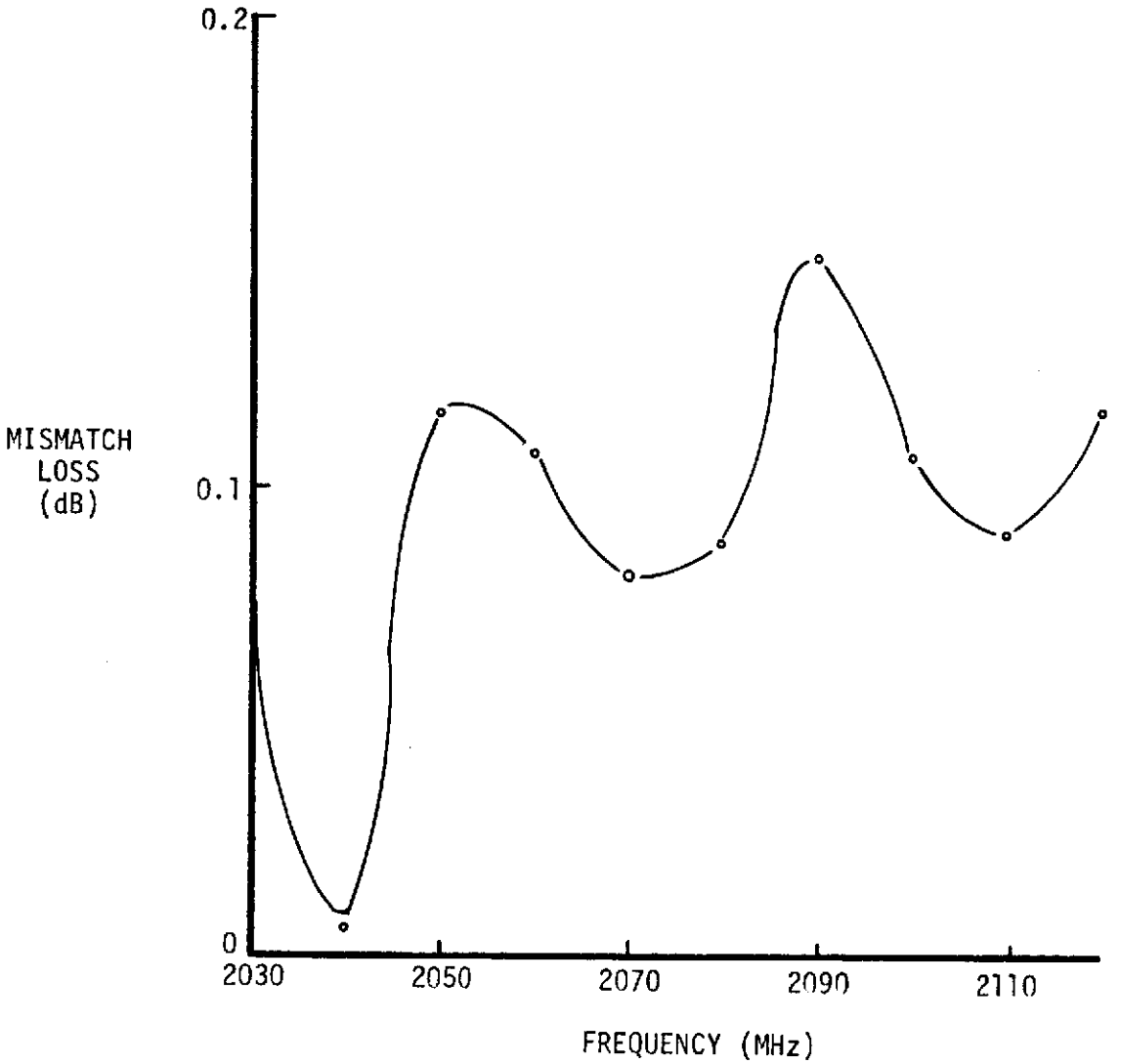

Figure 5-32. Computed Mismatch Loss, Optimum Source For Low Noise Performance

Design of the complete 3-stage configuration was typically conducted as follows:

- Gain circles on the impedance plane were generated for each stage (i.e., as a function of collector bias current) utilizing the HP 9820A calculator, the HP Microwave Pac software, and S-parameters previously measured. Gain circles typical of the first stage (Ic=7mA) are shown in Figure 5-33. The input and output gain circles converge to respective points which achieve maximum gain (G_{max}) identified as Γ_{ms} (reflection coefficient of conjugate input match) and Γ_{ml} (reflection coefficient of conjugate output match). The gain circles denote available gain when the device is terminated in impedances other than conjugate matches.

- For minimum noise figure, the source impedance presented to the AT4641 is identified as Γ_{opt} and it can be seen from Figure 5-33 that the resulting gain will be approximately 11.7 dB. This gain is achieved, however, only if the device is terminated in Γ'_{ml}. This represents a conjugate output match for the "new" source impedance Γ_{opt}, and deviations from this load can be analyzed through the use of the gain circles around Γ'_{ml}. These circles are specified as negative gain (loss) and are referenced to the maximum obtainable gain for Γ_{opt}, 11.7 dB.

- These gain circles are utilized to specify the circuit topology and approximate element values.

- The overall amplifier topology is specified on an optimization program and computer-aided design techniques are utilized to achieve a design which best meets all requirements.

The requirements established for the low-noise amplifier are shown in Table 5-11 and are compared against the computer optimized circuit. Actual performance data measured on the low-noise amplifier is shown in Figure 5-34.

This amplifier is shown schematically in Figure 5-26. The configuration was realized through definition of microstrip elements on 0.025-inch thick alumina substrate material using thin-film techniques. All bypass capacitors and the input and output blocking capacitors are chip components soldered in place; the DC blocking capacitors between stages are beam-lead components.

The bias stabilization circuitry utilizes chip resistors and is fabricated on a separate alumina substrate. This complete physical separation of RF and DC circuitry optimizes the assembly process and results in a cost-effective approach to increasing the overall circuit assembly yield; yields associated with the RF section are completely independent of DC circuit yields.

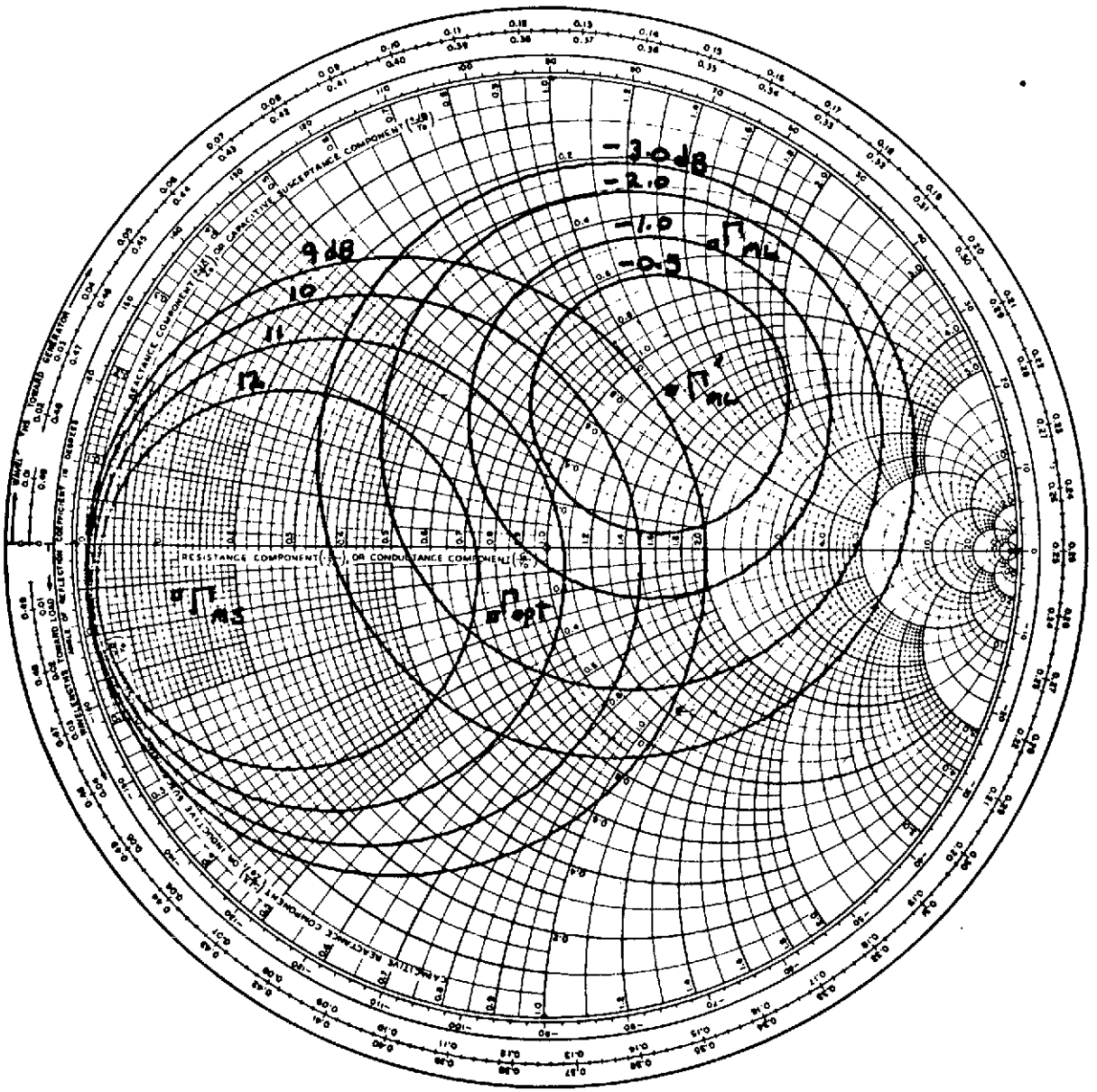

Figure 5-33. Source and Load Gain Circles, AVANTEK AT-4641 Low Noise Transistor, V_C = 10V, I_C = 7 mA

Table 5-11. Low Noise Amplifier, SPACS I Module

Parameter	Requirement	Results
Gain	33 dB, Typ	33 dB, Typ[1]
Noise Figure		
@ 2046 MHz	-	3.45 dB, Typ[2]
@ 2106 MHz	-	3.35 dB, Typ[2]
Bandwidth	2030 - 2120 MHz	1970 - 2170 MHz
Supply Voltage	12 Volt	12 Volt
Current Drain	30 mA	37 mA
Phase Linearity (Within required Bandwidth)	± 5 Degrees	± 1 Degree

1 Gain before receiver was tuned to optimize duplexed operation; gain increased above this value after tuning LNA/filter interface to optimize transmit frequency rejection

2 LNA was optimized for lowest noise figure when interfaced with combline filter impedance characteristic; calculated minimum noise figure of 3-stage amplifier is 3.0 dB, when interfaced with filter

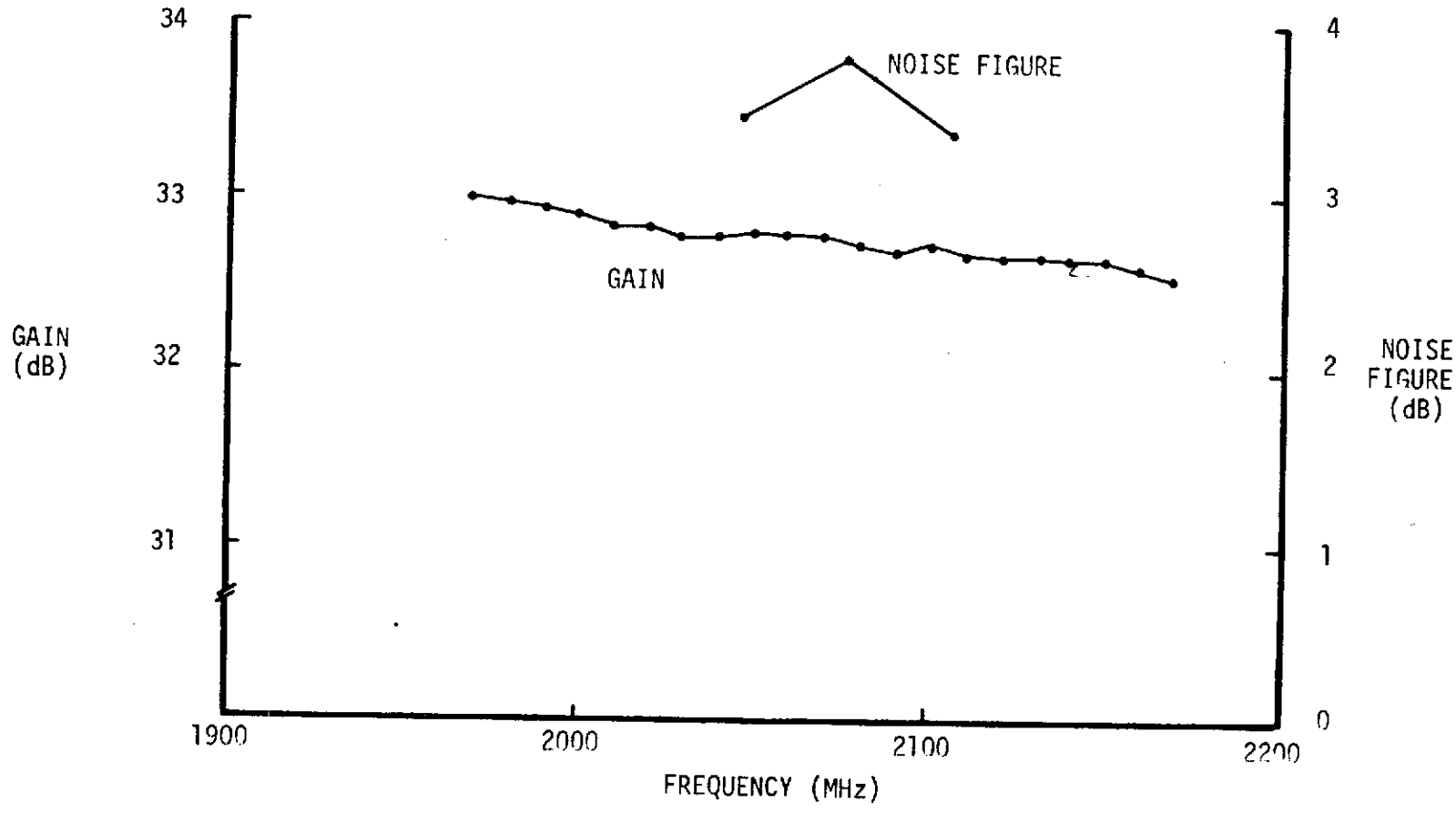

Figure 5-34. Low Noise Amplifier Performance

7. Receive Phase Shifter Design

The electronic phase shift circuit utilized by the module receiver is a 3-bit line-length type phase shifter similar in design to the one previously discussed in Section V.A.1, Transmit Phase Shifter Design. As in the transmit section, this phase shifter was also first demonstrated in the AESPA module (Contract No. NAS8-25847, Marshall Space Flight Center). Performance of that particular phase shifter, fabricated with beam-lead components, is shown in Table 5-12. This circuit was reconfigured with minor changes to accept the beam-lead components, to conform to the inherent physical requirements of the SPACS I module, and to be optimum for the center frequency (2074 MHz) of the SPACS receive bandpass.

Actual performance data recorded on the receive phase shifter integrated into the breadboard module is shown in Table 5-13. Circuit physical size is 0.600 x 1.200 x 0.025 inches and construction techniques are identical to those discussed in Section V.A.1.

8. Phase Shifter Logic

The logic circuitry which is used to accept phase shift commands and to set the appropriate phase bit position for each module transmitter and receiver is shown in the block diagram of Figure 5-35. This basic logic configuration was first demonstrated in the AESPA module (Contract No. NAS8-25847, Marshall Space Flight Center).

This configuration was designed to minimize power and weight while maximizing reliability by using fewer integrated circuit chips and interconnections. Reliability is further enhanced by the parallel transfer of phase data from the processor to the module. Serial transfer requires one clock per bit, while parallel transfer only requires one clock per 3-bit word. Consequently, the probability of noise interaction is decreased by a factor of 3 with the parallel approach. This configuration also allows the addition of offset phase capability. Optional jumpers, denoted by the dotted lines in Figure 5-35, are used to select the offset bit weight thereby modifying all phase shift values at the SN54LS83 adder before they are stored in the SN54L98 storage register. This phase offset capability may be used as a "gross" frequency-independent phase adjust for the phase characteristics of the transmitter and receiver in each module. Since each module has a phase shifter and logic circuit associated with both transmitter and receiver, this allows maximum flexibility in establishing phase characteristics for phased array applications.

Each logic circuit utilizes chip integrated circuits and chip resistor components solder mounted to a metalized alumina substrate. The interconnect pattern is photolithographically defined and processed using thin-film technology.

Table 5-12. Phase Shifter Performance, Insertion Loss, VSWR and Phase Error as a Function of Bit Position

Bit	Commanded Phase (Degrees)	Insertion Loss (dB)	VSWR (Ratio)	Phase Error (Degrees)
0	0	1.44	1.17	-
1	45	1.81	1.20	+ 4.4
2	90	1.80	1.25	+ 4.8
3	135	1.87	1.09	+ 7.9
4	180	1.62	1.01	+ 3.8
5	225	1.95	1.16	+ 7.6
6	270	1.75	1.34	+ 8.3
7	315	1.85	1.21	+13.1

FREQUENCY = 2075 MHz

Table 5-13. Receive Phase Shifter Performance, Breadboard Module

Bit	Commanded Phase (Degrees)	Insertion Loss (dB)	VSWR (Ratio)	Phase Error (Degrees)
0	0	1.50	1.076	-
1	45	1.74	1.189	-0.7
2	90	1.71	1.356	+1.7
3	135	1.63	1.405	-2.0
4	180	1.51	1.212	-2.8
5	225	1.65	1.310	-4.8
6	270	1.46	1.186	-4.9
7	315	1.54	1.23	-8.6

FREQUENCY = 2080 MHz

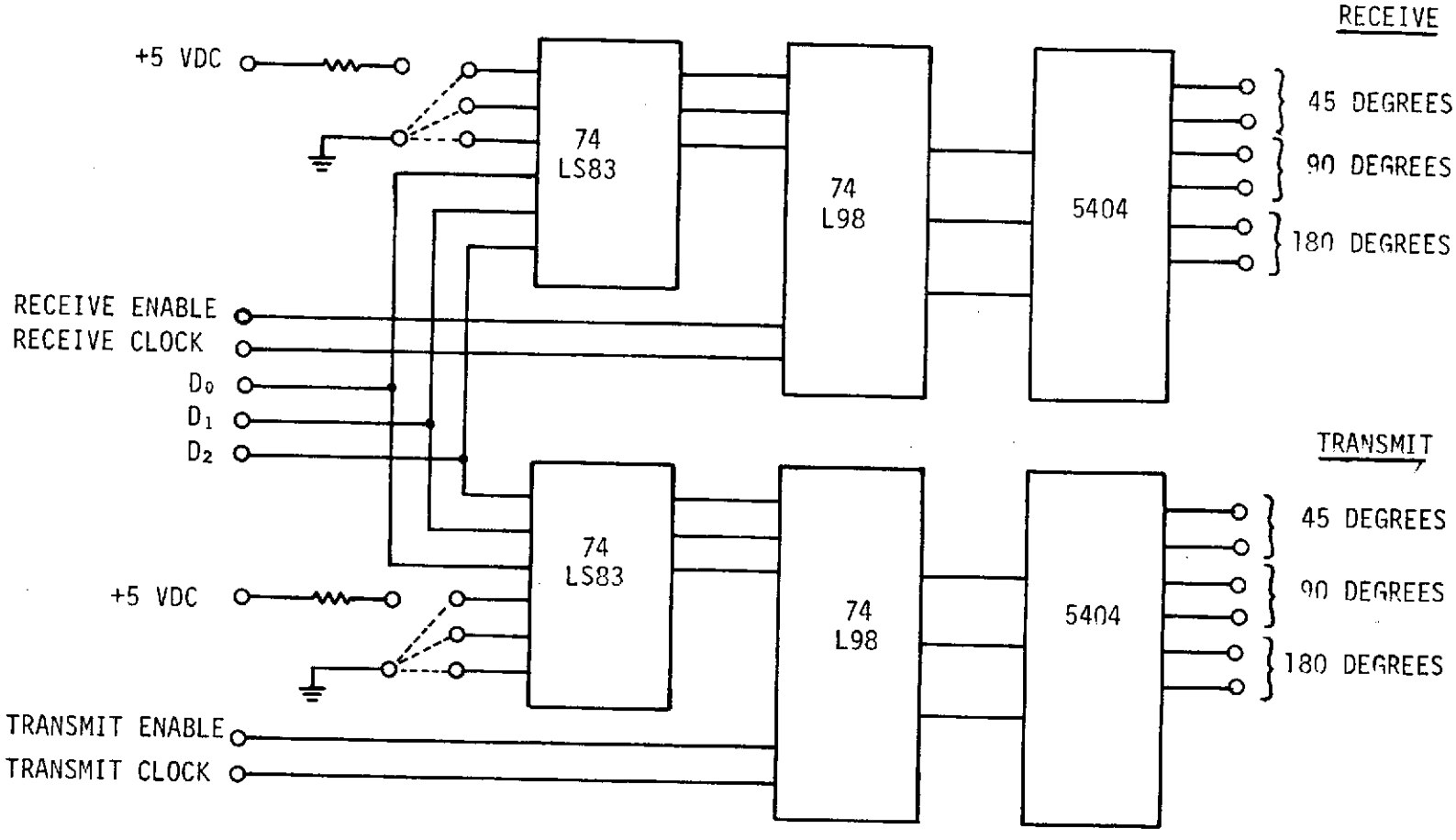

Figure 5-35. Phase Shift Logic, SPACS I Module Block Diagram

A complete schematic of the phase shifter logic is shown in Figure 5-36. The physical size of the transmitter logic circuit is 0.300 x 1.200 x 0.025 inches. The physical size of the receiver logic circuit is 0.425 x 1.200 x 0.025 inches, it being slightly wider to accomodate an RF transmission line to direct the received signal from the duplexer into the comb-line filter. Each logic circuit contains all components necessary for proper biasing of the phase shifter diodes, thereby separating the DC biasing section of the phasor from the RF section.

9. Design Tradeoffs

Module design tradeoffs were evaluated throughout the development phase on a continuing basis and were notably in the following areas:

- Receive bandpass filter
- Transmit bandpass filter
- Phase shifter components

The receive bandpass filtering constraints presented basic physical limitations in order to simultaneously achieve the required rejection and receiver noise figure. Module weight and size were considered of prime importance for an application such as the SPACS I area, but were somewhat compromised in order to incorporate a filter which would meet both noise figure and rejection requirements.

Transmit bandpass filters were fabricated on two different thicknesses of alumina substrate material, 0.025 and 0.040 inch. The thinner material is considered an industry-standard for microwave integrated circuit (MIC) work. Evaluation of a filter design on this material, however, resulted in passband insertion losses somewhat higher than originally established as acceptable. Rather than increase the power amplifier output power a corresponding amount (thus decreasing transmitter reliability), the decision was made to fabricate the filter on the 0.040-inch alumina. This optimized transmitter reliability, met the rejection requirements, and allowed sufficient transmitter power to adequately meet the antenna EIRP requirements.

Phase shifter circuits originally evaluated utilized chip PIN diodes and chip capacitors fabricated from metallized titanate materials. These components represented a minimum materials cost, but also had several disadvantages. Die attaching (preform method) 12 chip diodes and solder mounting 12 chip capacitors per phase shift network would represent substantial labor costs subject to the rather poor yield of such an assembly procedure. A minimum of one bond wire per component (24 total) would also be required to complete component integration. These bond wires present significant reactances which degrade phase shifter performance and performance repeatability. Beam-lead components represent an initial higher cost in the bill of materials, but possess the inherent advantages of ease of mounting, minimum parasitics, and improved circuit assembly yields.

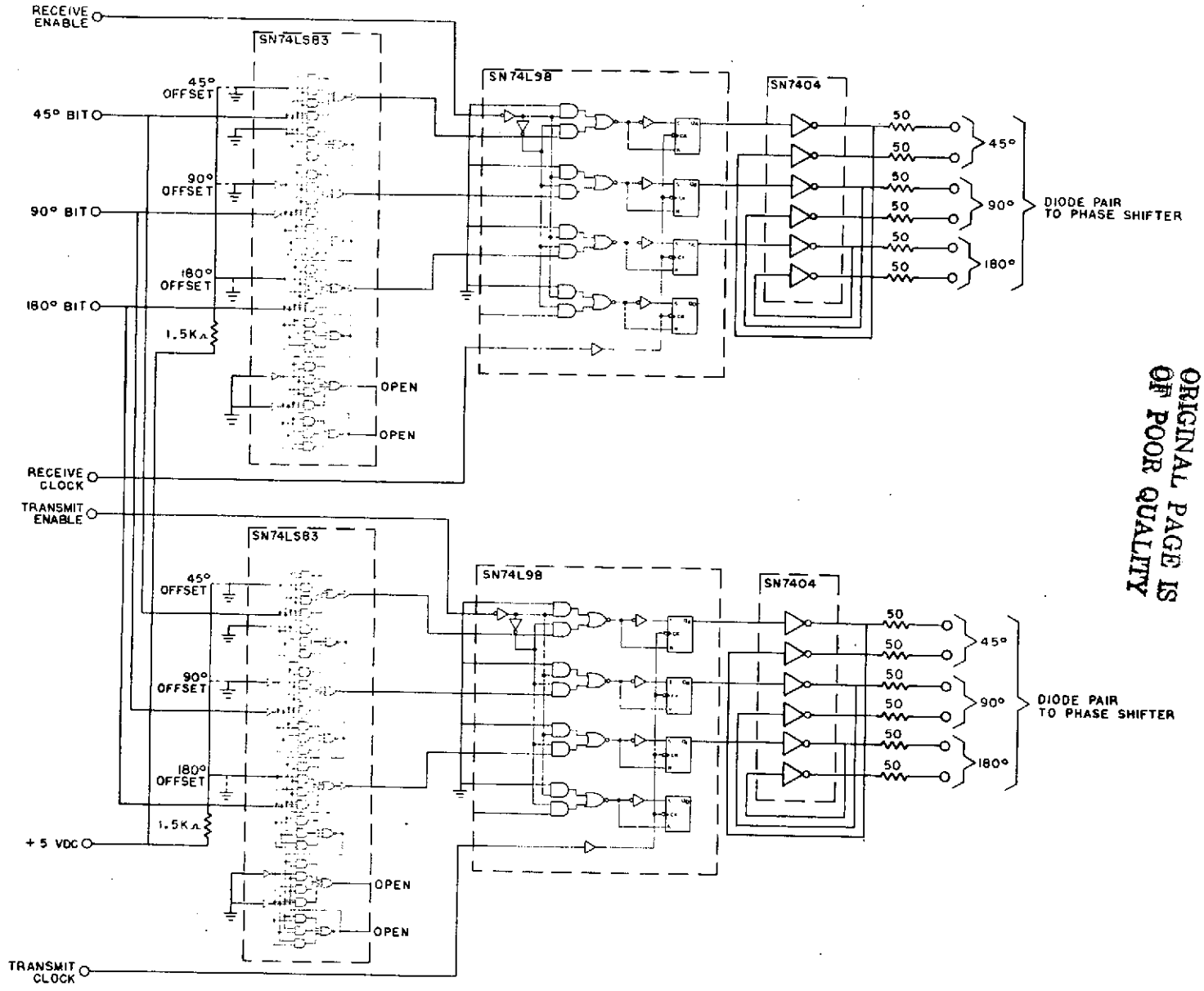

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Figure 5-36. Phase Shift Logic, SPACS I Module, Detailed Electrical Schematic

Beam-lead components were then used exclusively on both phase shifter circuits in an effort to optimize yields and to minimize assembly costs associated with these circuits.

B. BREADBOARD MODULE EVALUATION

1. Measurement Methods

A significant portion of the RF measurements made on the SPACS I breadboard module were performed using the Hewlett-Packard Automatic Network Analyzer. By using this computer-directed test facility, accurate initial calibration and correction of all subsequent measurements is insured over a broad frequency range. This hardware can typically conduct multiple measurements and store such information as gain, phase, group delay, reflection coefficient magnitude and angle, VSWR, two-port parameters, etc., faster than it can be reproduced by the teletype printer. A copy of the module acceptance test procedure and test data is included in Appendix B for reference purposes.

The HP 8746B Test Set was utilized for measurement of the module receiver section. This particular test set allows the receiver RF input level to be set in the range of -20 to -60 dBm to prevent overdriving the low noise amplifier and recording test data in a non-linear range of operation. Signal level is set at the touch of a button, the test set is calibrated at that setting, and data recorded. The inherent advantage in this approach is that no attenuator is required external to the test set to reduce the signal level at the antenna port of the module. Were this approach used, antenna port VSWR would be masked by the return loss of the external attenuator.

The HP 8745A Test Set was utilized for measurement of the module transmitter section. In addition, special high-power hardware and software developed by Texas Instruments, Inc. Advanced Systems Department allowed automated testing of the transmitter section at RF input levels of +12 to +14 dBm. Calibration of the test set and testing at 88 unique frequency/power level points is representative of the present capability of this hardware.

Noise figure measurements were conducted within a "screen-room" area using the AIL Model 75 Precision Automatic Noise Figure Indicator and a Model 7010 Gas Tube Noise Source calibrated against a "standard" noise source characterized by the National Bureau of Standards.

Receiver gain compression and duplex operation testing were conducted manually at a test set established within the engineering laboratory area.

2. Transmitter Data

Transmitter data obtained on the final breadboard module is shown graphically in the following figures. Transmitter output power as a function of phase bit position, RF input power level, and frequency is shown in Figures 5-37, 5-38, and 5-39. Transmitter insertion phase as a function of phase bit position, RF input power level, and frequency is shown in Figures 5-40, 5-41, and 5-42. Transmitter input port VSWR as a function of phase bit position, RF input power level, and frequency is shown in Figures 5-43, 5-44, and 5-45. The primary performance goals are compared with measured results in Table 5-14.

3. Receiver Data

Receiver data obtained on the breadboard module with the automatic network analyzer is shown graphically in the following figures. Receiver gain as a function of phase bit position and frequency is shown in Figure 5-46. Receiver insertion phase as a function of phase bit position and frequency is shown in Figure 5-47. Antenna port VSWR as a function of phase bit position and frequency is shown in Figure 5-48. Typical performance results are summarized in Table 5-15 and are compared to the receiver design goals.

Receiver noise figure and gain compression were measured at three frequencies within each spread-spectrum bandpass and at one frequency centered within the overall receiver bandwidth. These results are summarized in Table 5-15 and are compared to the receiver design goals.

4. Module Duplexed Operation

During module acceptance testing, duplexed operation of the module was evaluated by transmitting into a 1.6:1 VSWR antenna load and allowing the reflected signal to enter the receiver. The receiver output level at the transmit frequency was noted and compared to the compression point (-1 dB gain reduction) of the receiver. These results are summarized in Table 5-16. Questions regarding the validity of such a test resulted in further testing for fully-duplexed operation.

The test set shown in Figure 5-49 was utilized to conduct an evaluation of the module in the fully duplexed mode. With the transmitter initially turned off, a spectrum analyzer was used to establish a -40 dBm receive signal (2041.9 MHz) at the module antenna port. The receiver output was then monitored and an output level of -6 dBm (implying a receiver gain of 34 dB) was noted. When the transmitter was then enabled (2217.5 MHz) and operated into the 1.6:1 VSWR antenna load, the receiver output levels were again noted.

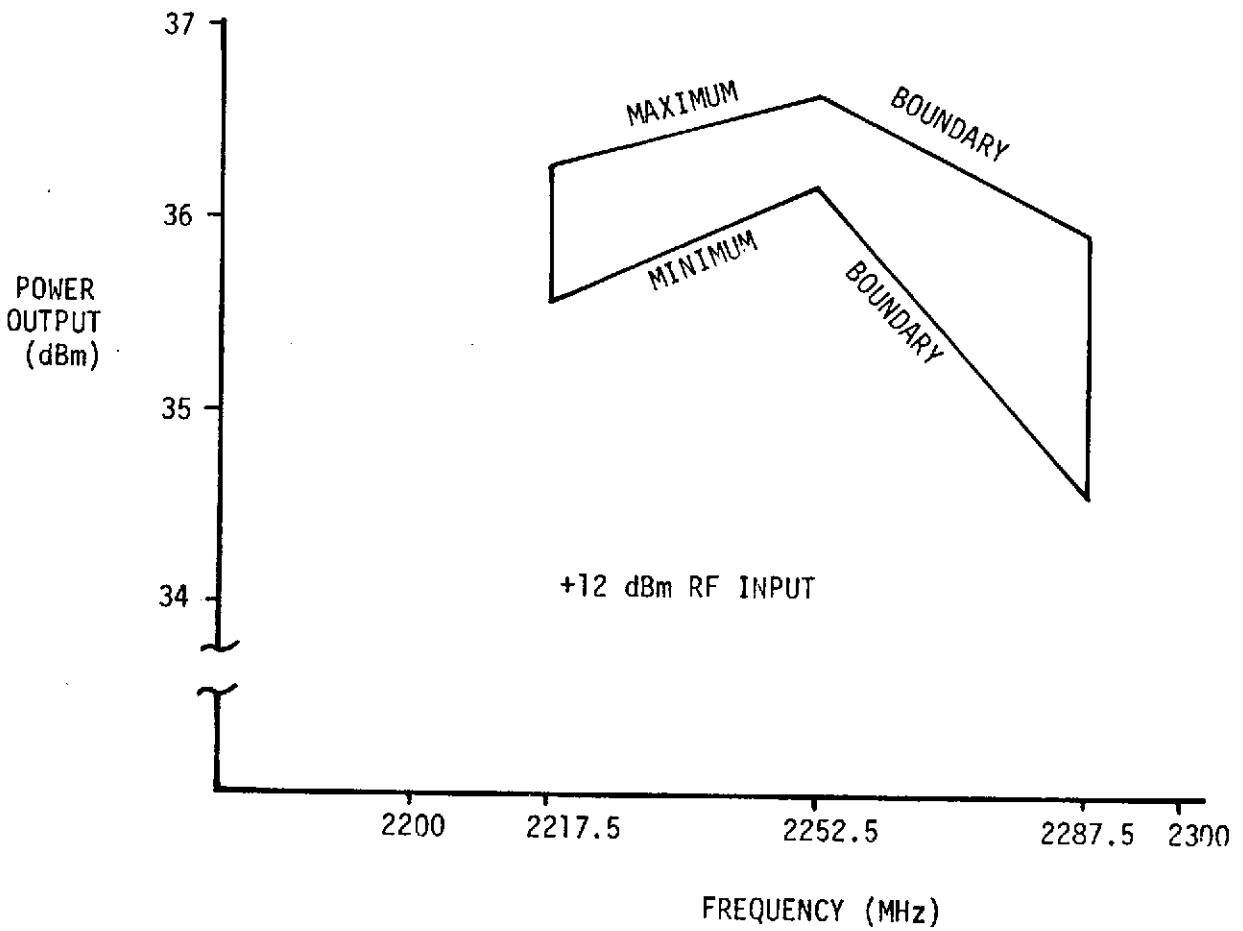


Figure 5-37. Transmitter Power Output Boundaries, +12 dBm RF Input, All Phase Bits

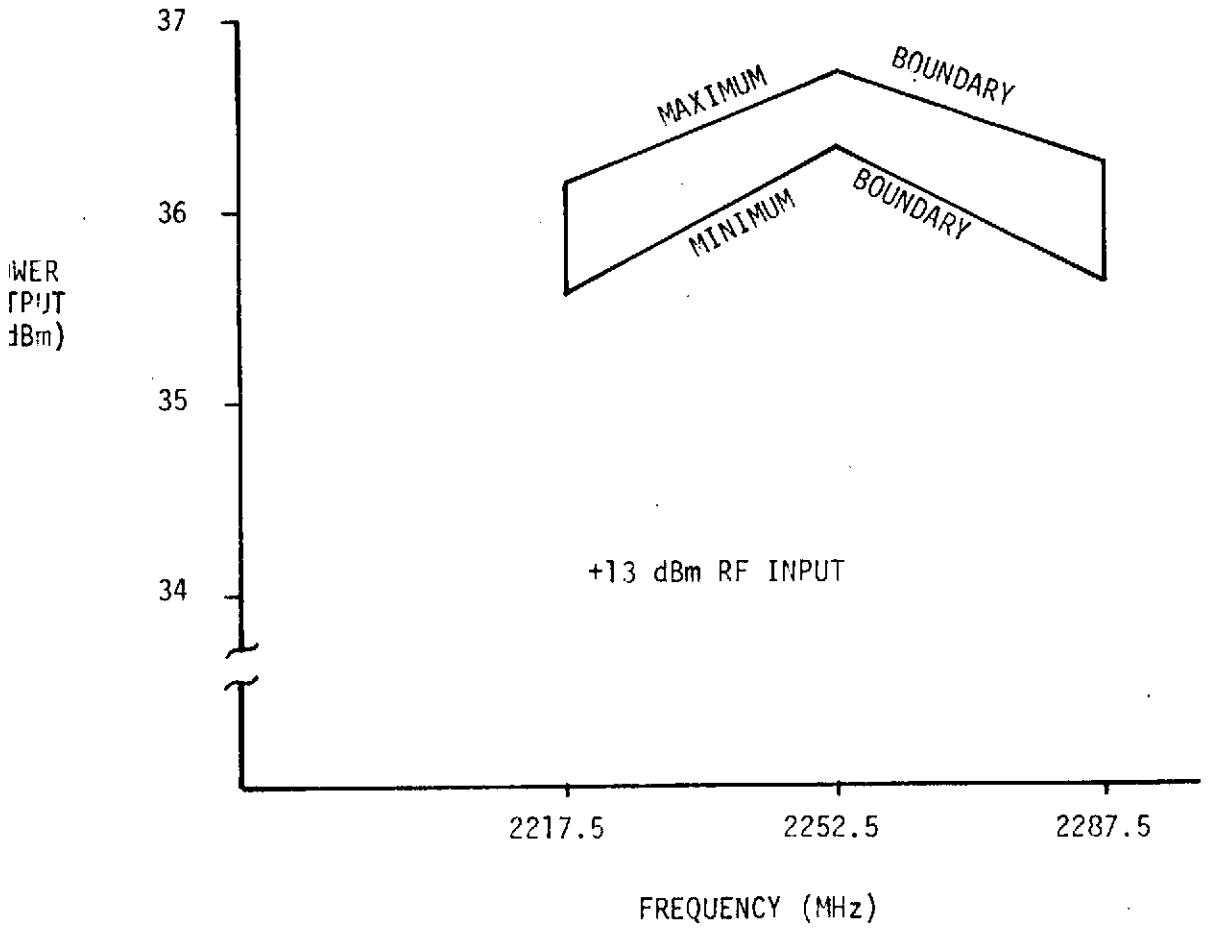


Figure 5-38. Transmitter Power Output Boundaries, +13 dBm RF Input, All Phase Bits

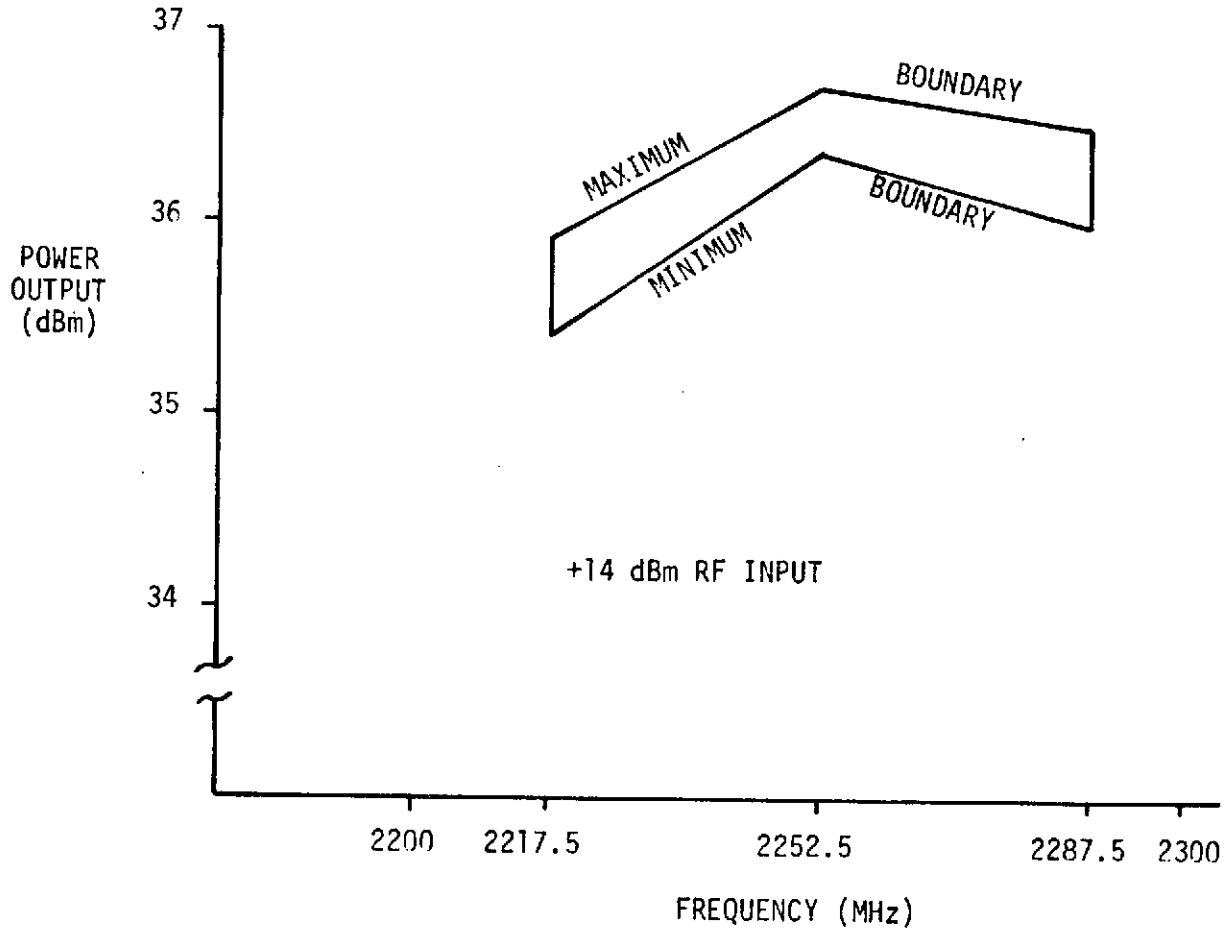
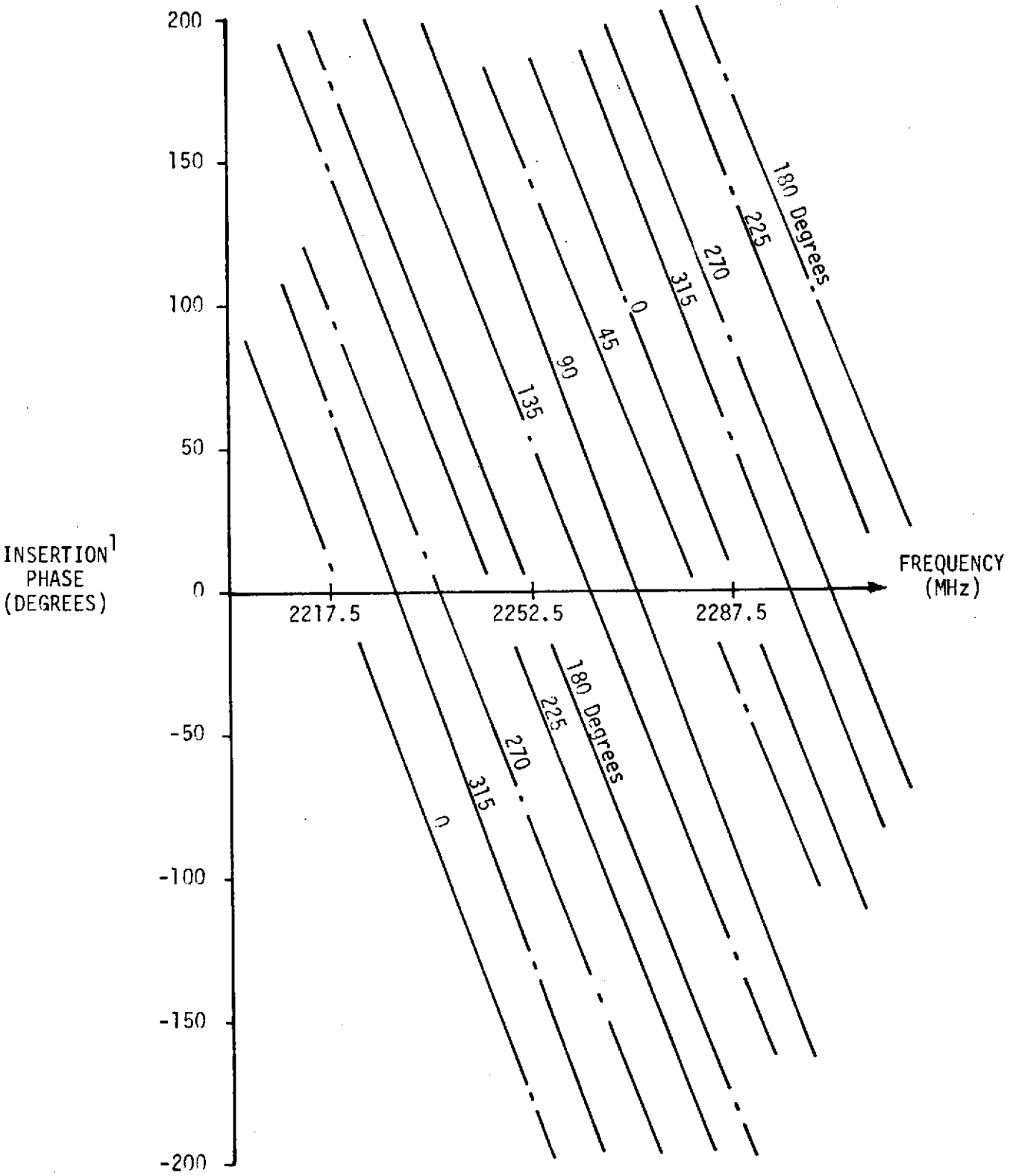
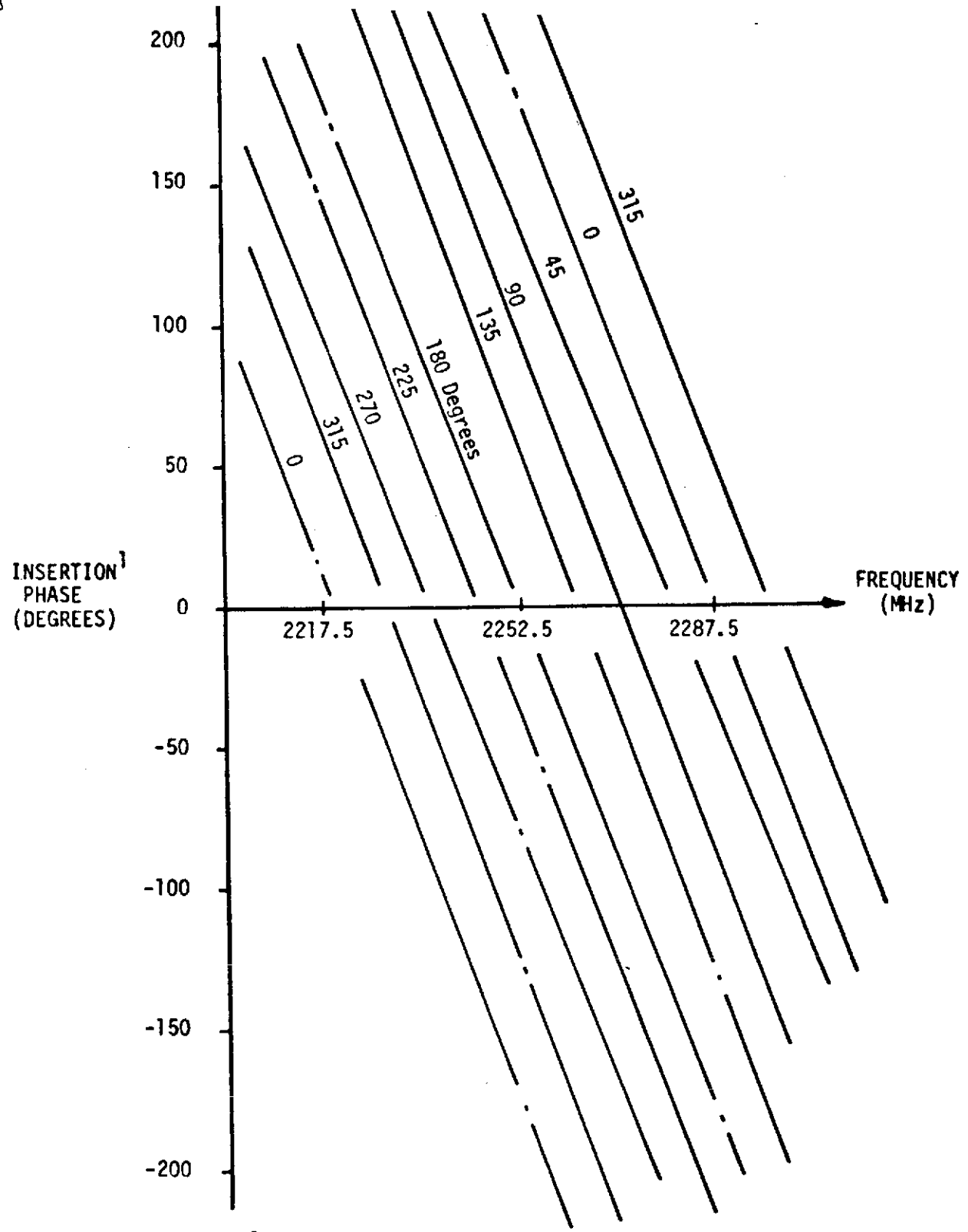


Figure 5-39. Transmitter Power Output Boundaries, +14 dBm RF Input, All Phase Bits



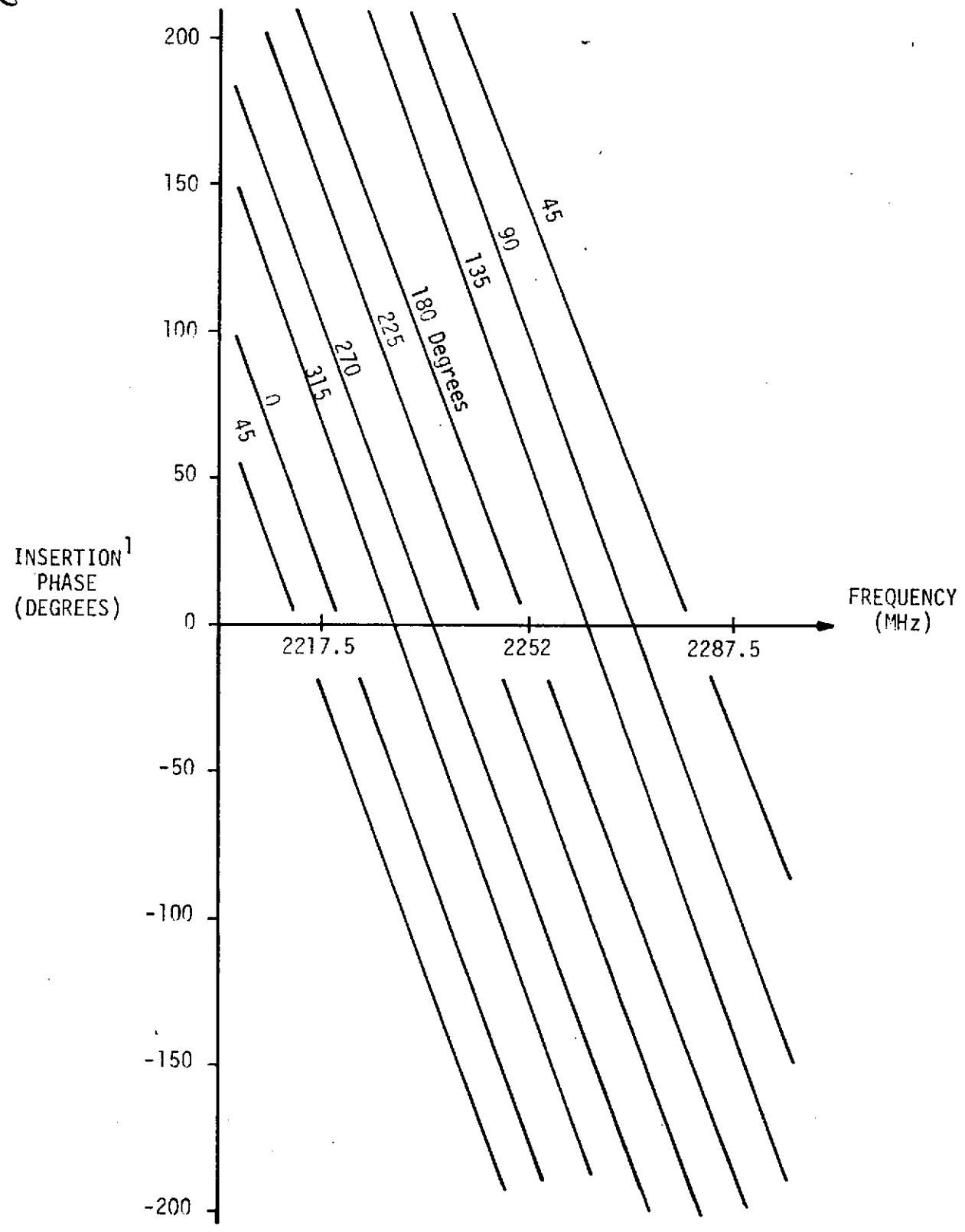
[1] Includes Insertion Phase of 26 dB Attenuator For Gain Offset

Figure 5-40. Transmitter Phase, +12 dBm RF Input, All Phase Bits



[1] Includes Insertion Phase of 26 dB Attenuator For Gain Offset

Figure 5-41. Transmitter Phase, +13 dBm RF Input, All Phase Bits



[1] Includes Insertion Phase of 26 dB Attenuator For Gain Offset

Figure 5-42. Transmitter Phase, 14 dBm RF Input, All Phase Bits

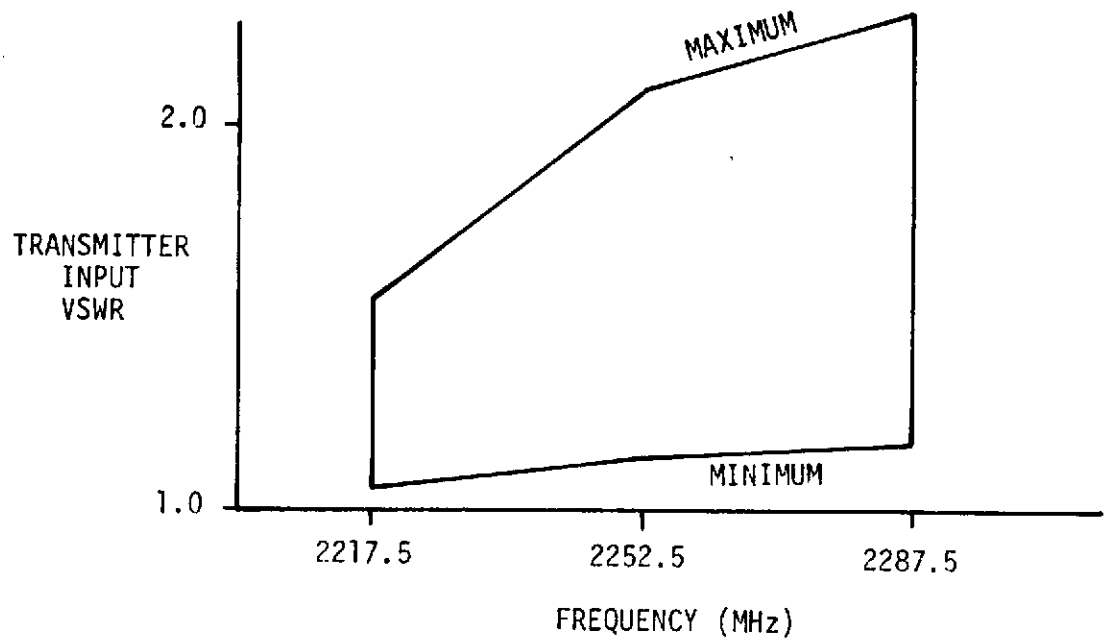


Figure 5-43. Transmitter Input VSWR Boundaries, +12 dBm RF Input Level, All Phase Bits

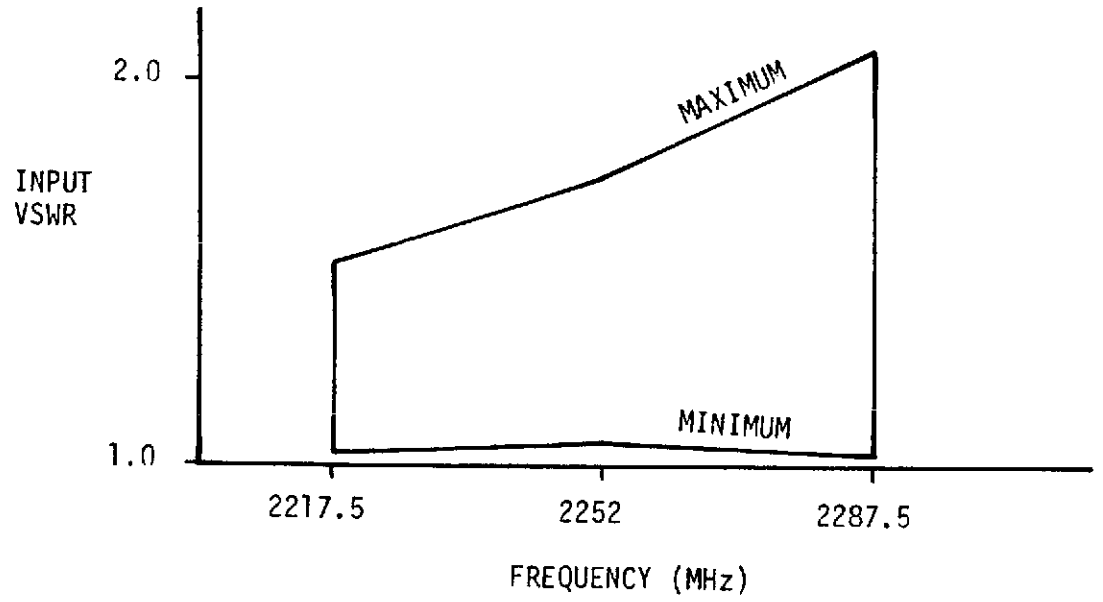


Figure 5-44. Transmitter Input VSWR Boundaries, +13 dBm RF Input Level, All Phase Bits

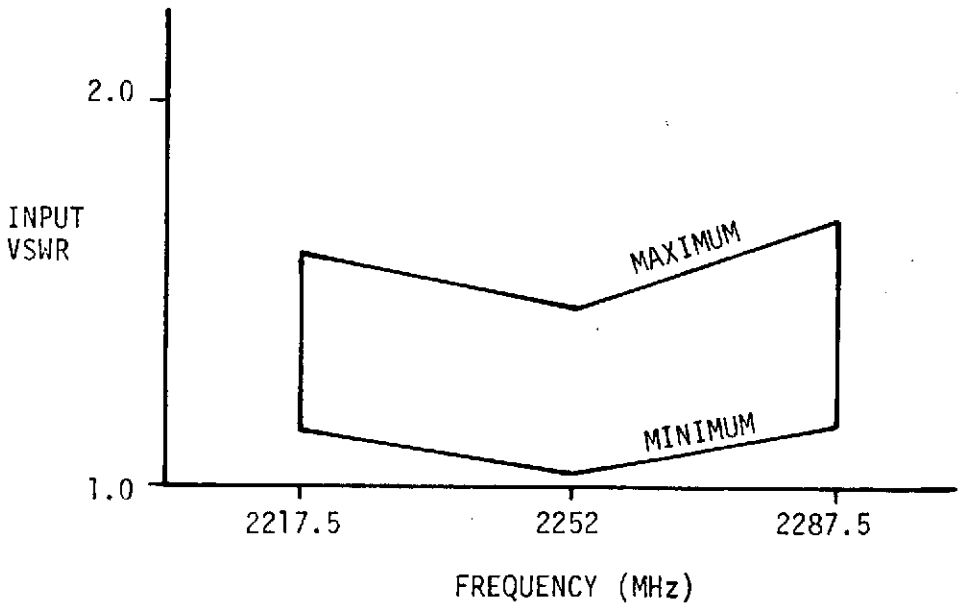


Figure 5-45. Transmitter Input VSWR Boundaries, +14 dBm RF Input Level, All Phase Bits

Table 5-14. Performance Summary SPACS I Transmitter

Parameter	Design Goals	Measured Values
Instantaneous Band width	2217.5 - 2287.5 MHz	2217.5 - 2287.5 MHz
Power Gain (Module input to antenna port)	20 dBm Min	23 dB, Typ
Power Output	+35 dBm, Typ	+35.5 dBm @ 2217.5 MHz +36.5 dBm @ 2252 MHz +35.5 dBm @ 2287.5 MHz
Supply Voltages	+ 5 V, Typ +12 V, Typ +24 V, Max	+ 5 VDC +12 VDC +22 VDC
Current Drain		
@ + 5 VDC	-	37 mA, Typ
@ +12 VDC	50 mA, Typ	6 mA, Typ
@ +24 VDC	600 mA, Typ	900 mA @ 2217.5 MHz 900 mA @ 2252 MHz 750 mA @ 2287.5 MHz
RF Power Input Level	+15 to +17 dBm Maximum	+12 to +14 dBm

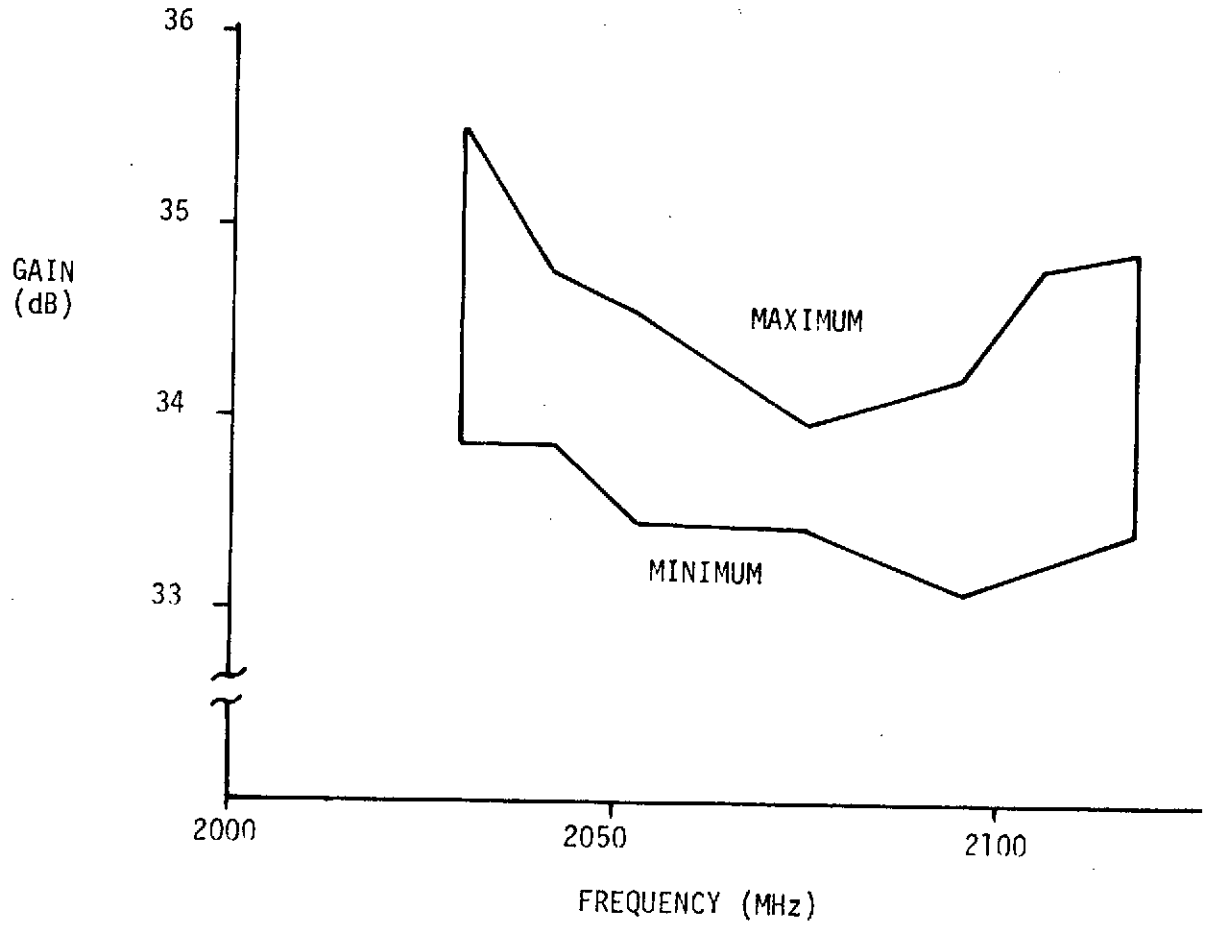


Figure 5-46. Receiver Gain Boundaries, -40 dBm RF Input, All Phase Bits

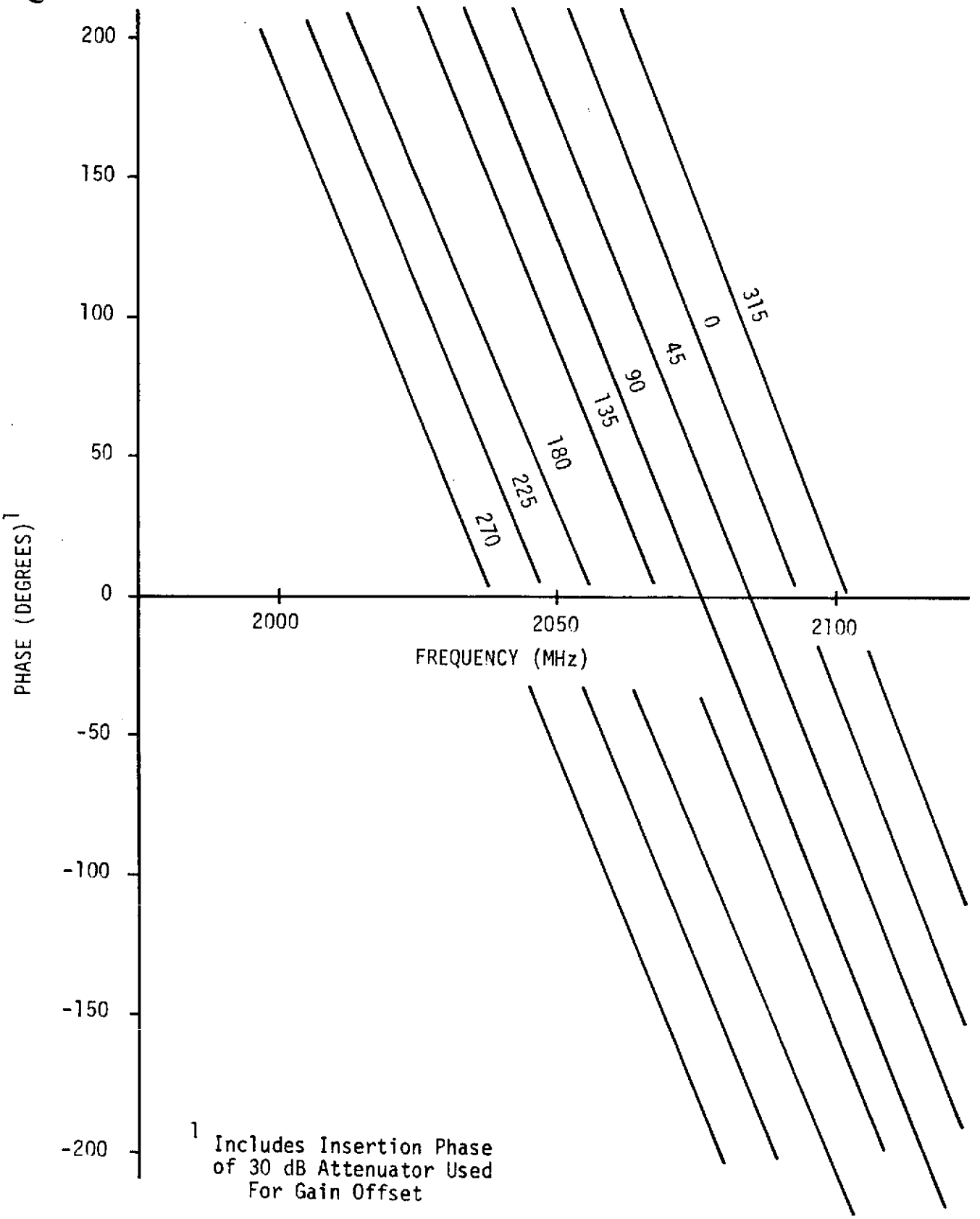


Figure 5-47. Receiver Phase, -40 dBm RF Input, All Phase Bits

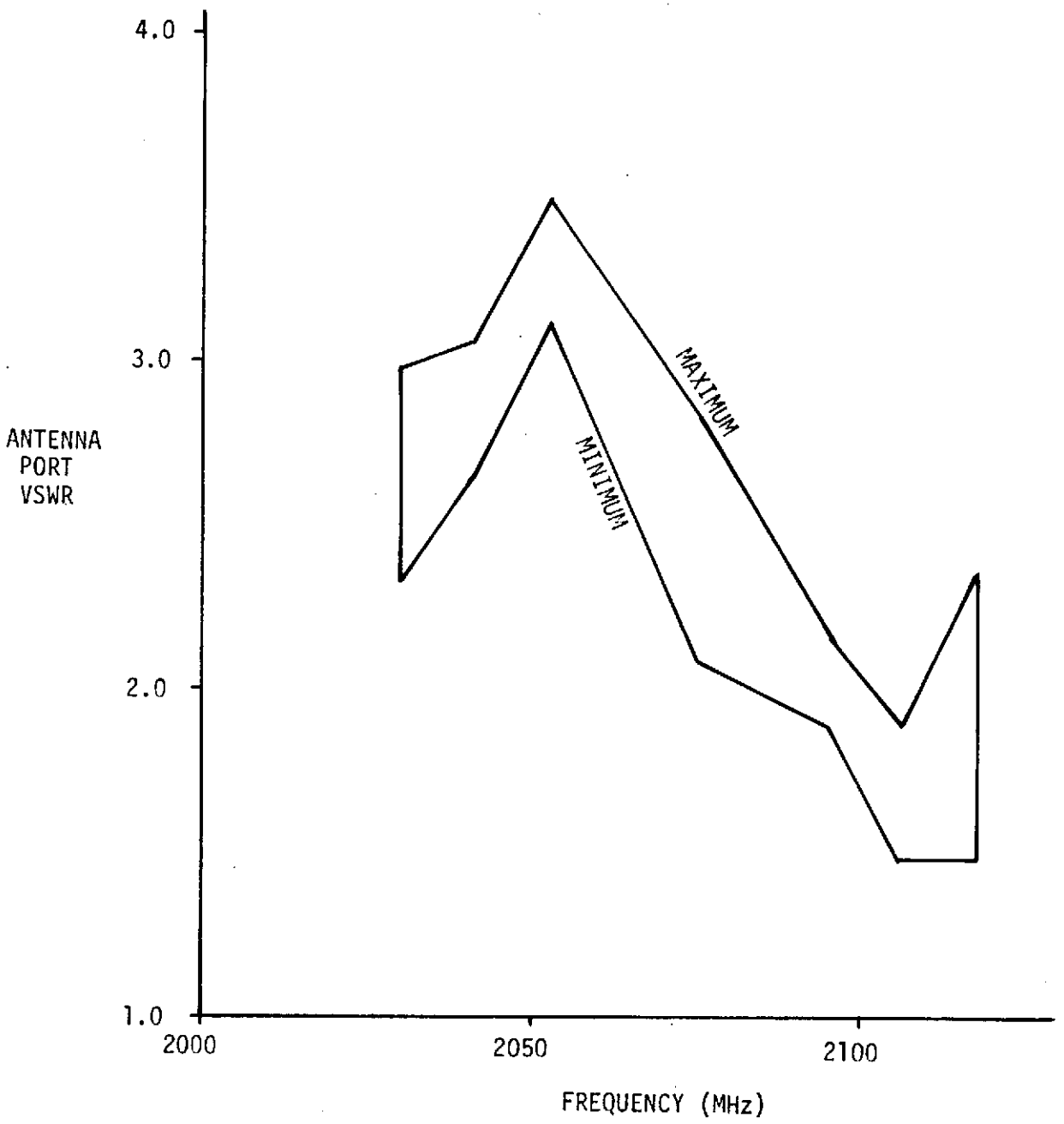


Figure 5-48. Receiver Antenna Port VSWR, -40 dBm RF Input, All Phase Bits

Table 5-15. Perfromance Summary, SPACS I Receiver

Parameter	Design Goals	Measured Values
Instantaneous Bandwidth	2030.9 - 2117.4 MHz	2030.9 - 2117.4 MHz
Power Gain (Antenna port to module output)	25 dB, Min	33 dB, Typ
Noise Figure	4.87 dB[1], Max 5.33 dB[2], Max	5.0 dB @ 2041.9 MHz 4.8 dB @ 2074 MHz 4.1 dB @ 2106.4 MHz
Output 1 dB Gain Compression Point	+10 dBm, Min	+ 9.75 dBm @ 2041.9 MHz +10.3 dBm @ 2074 MHz +10.45 dBm @ 2106.4 MHz
Supply Voltages	+ 5 VDC +12 VDC	+ 5 VDC +12 VDC
Current Drain @ 5 VDC @ 12 VDC	 - 30 mA, Typ	 37 mA, Typ 37 mA, Typ

1 Design Goal

2 Contract Requirement

Table 5-16. Module Duplex Evaluation, Final Acceptance Test

Frequency (MHz)	Output 1 dB Compression Point (dBm)	Transmit Signal Level from Receiver Under Duplex Operation (dBm)
2041.9	+ 9.75	-
2074.15	+10.3	-
2106.4	+10.45	-
2217.5	+10.3	+8.0
2252.5	+ 8.5	-2.0
2287.5	-12.6	-8.2

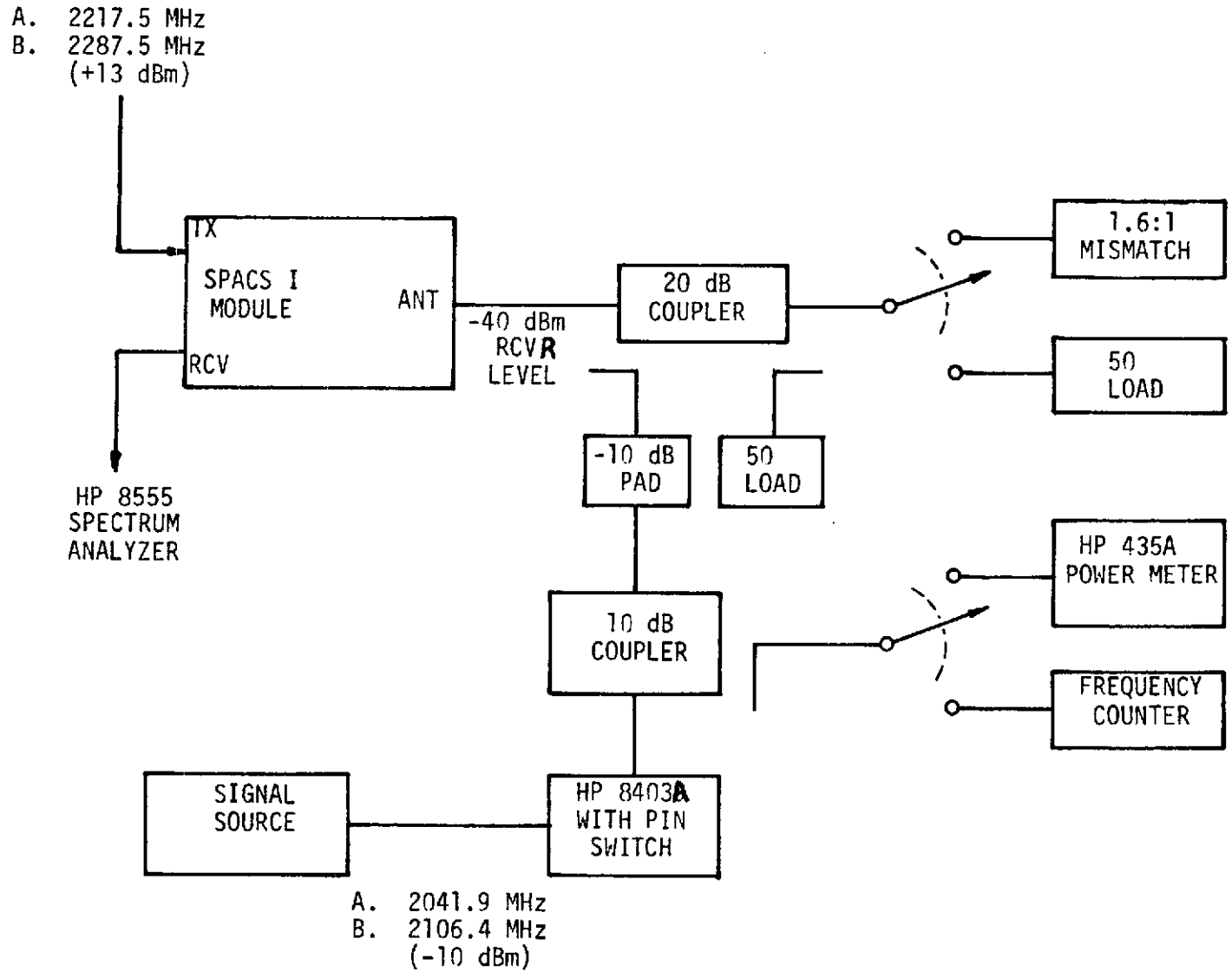


Figure 5-49. Module Duplex Test Set, SPACS I

Output level at the transmit frequency was +10 dBm and at the receive frequency, -8 dBm. This indicated slight compression of the receiver and a resulting 2 dB degradation in receiver gain which will not affect array performance since receiver gain is still greater than 30 dB. The same test was repeated at the upper frequency band (transmit at 2287.5 MHz, receive at 2106.4 MHz) and no detectable degradation in receiver gain was noted. These results are summarized in Table 5-17.

An evaluation of intermodulation distortion was also conducted under fully duplexed operation. The lower band test described above was repeated with the 1.6:1 VSWR load replaced by a load VSWR less than 1.05:1. The module was fully duplexed and other frequency products were observed to be greater than 40 dB below the receiver carrier frequency level. The 50 ohm load was replaced with the 1.6:1 VSWR mismatch and a frequency product (2390 MHz) was observed to be 22 dB below the receive carrier frequency. This represents a second-order intermodulation term produced by fully duplexed operation into a mismatch typically of the spiral antenna, but should not degrade the array performance. The intermodulation test was also repeated at the upper frequency band (transmit at 2287.5 MHz, receive at 2106.4 MHz). No intermodulation products greater than 40 dB below the receive carrier frequency were observed for either antenna port termination.

The module was also evaluated in the fully duplexed mode with pulsed modulation on the receive carrier frequency such that a sin x/x frequency spectrum was established with 4.6 MHz between second nulls. As viewed on a spectrum analyzer log display, no discernible difference was noted as the transmitter was switch on and off for the upper band channels. When the test was conducted on the lower band channels the only discernible change in the frequency spectrum was a small change in amplitude comparable to the 2 dB gain change noted in the initial duplex testing. Displays of this frequency spectrum change are shown in Figure 5-50. As can be seen in these pictures, no receiver distortion occurs for the transmitter-on under duplex operation. Hence, no phase information will be lost.

5. DC Power Budget

A DC power budget for the total module is included for reference and is summarized in Table 5-18. Current drain and required prime power is shown for two cases on the module transmitter; RF signal input present and no RF signal input present. The second and third stages of the power amplifier are operated class C and, therefore, do not require any bias current unless an RF input signal is present. The prime power required for the receive section is independent of power level for linear operation of the low noise amplifier.

6. Device Junction Temperature and Reliability

Active device junction temperatures have been calculated for typical module operating temperatures expected in the breadboard array system. These temperatures are based on typical power dissipation levels

Table 5-17. Performance Summary, Module Duplex Evaluation

Receive Level (dBm)		Transmit Level (dBm)		Freq (MHz)	Load VSWR
AT Antenna	AT Rcv Output	AT Antenna	AT Rcv Output	Xmit/Rcv	
-40	-6	-	-	Off/2041.9	1.6:1
-40	-8	> +35	+10	2217.5/2041.9	1.6:1
-40	-6	-	-	Off/2106.4	1.6:1
-40	-6	> +35	- 6	2287.5/2106.4	1.6:1

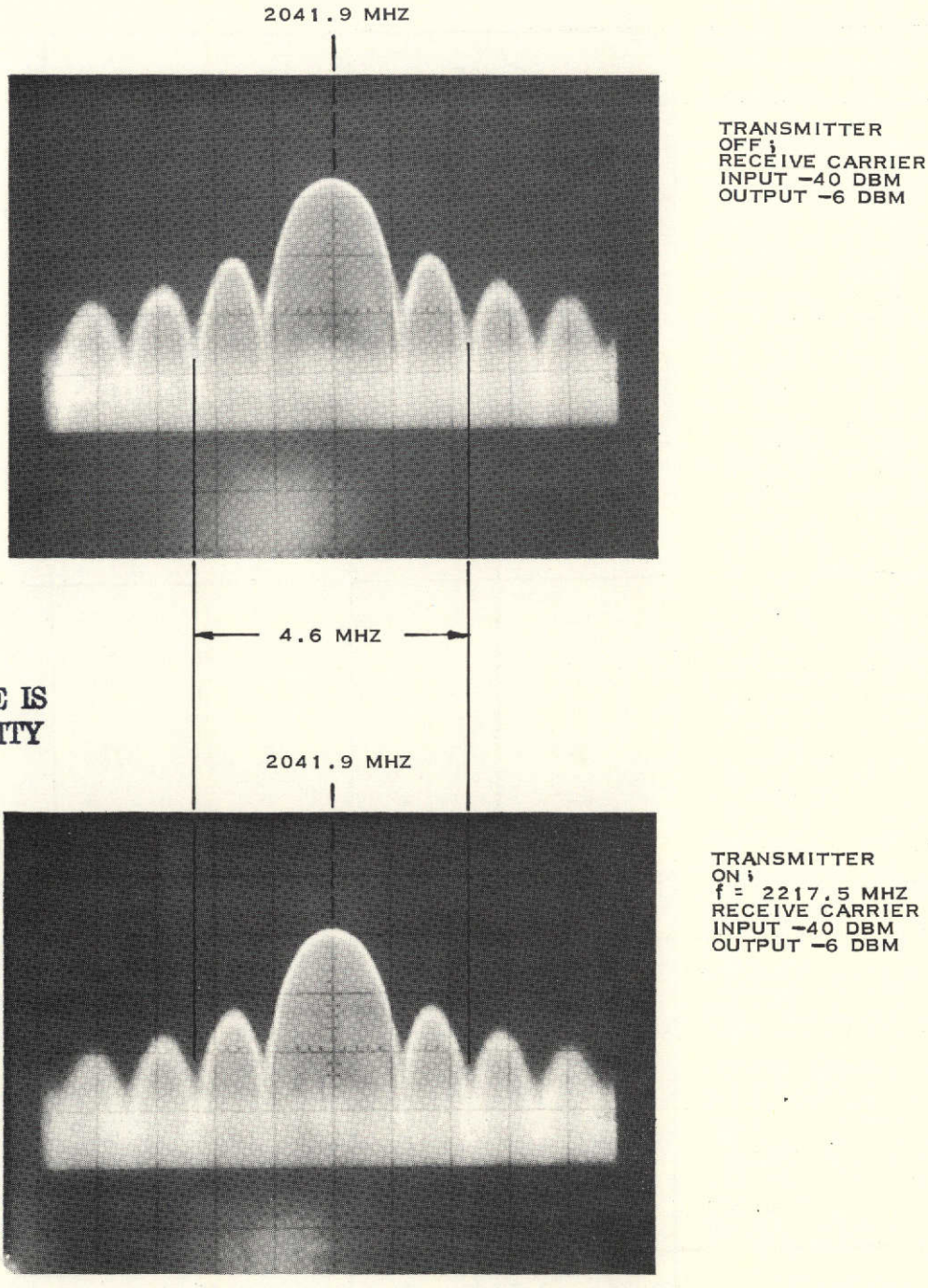


Figure 5-50. Amplitude-Modulated Frequency Spectrum Under Fully-Duplexed Operation

Table 5-18. DC Power Budget, SPACS I Module

	+5 VDC		+12 VDC		+22 VDC	
	Current (mA)	Power (W)	Current (mA)	Power (W)	Current (mA)	Power (W)
Transmit Section (No RF Signal Input)						
Power Amplifier, 1st Stage	-	-	6	.072	26	.572
, 2nd Stage	-	-	-	-	-	-
, 3rd Stage	-	-	-	-	-	-
Phase Shifter and Logic	37	.185	-	-	-	-
Transmit Section (RF Signal Input)						
Power Amplifier, 1st Stage	-	-	6	.072	26	.572
, 2nd Stage	-	-	-	-	120	2.64
, 3rd Stage	-	-	-	-	750	16.50
Phase Shifter and Logic	37	.185	-	-	-	-
Receive Section						
Phase Shifter and Logic	37	.185	-	-	-	-
Low Noise Amplifier, 1st Stage	-	-	7	.084	-	-
, 2nd Stage	-	-	10	.120	-	-
, 3rd Stage	-	-	20	.240	-	-
Total Power	0.37 W		0.52 W		19.71 W	

Total DC Power Per Module = 20.6 W

observed in the breadboard module and manufacturers recommended values for device thermal impedance. This data is summarized in Table 5-19. In the case of semiconductor components with a given contact metallization system, the operating junction temperature can be related to mean-time-to-failure through the use of calculated and/or measured data such as that shown in Figure 5-51. This figure contains calculated and measured reliability data on some typical RF power transistors such as the MSC4001 transistor used in the SPACS I transmitter. It is noted that for junction temperatures equal to or less than 140°C, mean-time-to-failure exceeds a calculated value of eight years and exceeds a measured value (obtained through reliability stress testing) of 50 years.

C. SUMMARY AND CONCLUSIONS

A transceiver module utilizing state-of-the-art microwave integrated circuit technology has been designed for fully-duplexed operation in an active element phased array communications antenna.

Module operational requirements and results of module electrical testing are summarized in Table 5-20.

The complete module circuitry is shown in Figure 5-52 and each unique circuit function is identified for reference purposes.

The overall module concept is completely compatible with the array requirements and meets or exceeds the original requirements established for a viable module design.

D. RECOMMENDATIONS FOR FUTURE IMPROVEMENTS OF FLIGHT MODEL

Specific areas of the present module configuration can be identified and considered for possible future improvement.

- Receive bandpass filter - As filter technology continues to progress, filters are presently being demonstrated at one-third the frequency of the SPACS I receiver band which are smaller and lighter than the SPACS I comb-line filter. These filters have a 2 dB passband insertion loss and rejection of 45 dB at a frequency located one and one-half times the 1 dB bandwidth above the filter center frequency. The percent bandwidth of the 1 dB points is 6.5%. This represents significant miniaturization capability and the technology might be applied to reduce module size and weight.

Table 5-19. RF Device Junction Temperature Summary

DEVICE	DISSIPATED POWER (W)	Θ_{js} (°C/W)	ΔT_{jmax} [1] (°C)	T_{jmax} [2] (°C)
Power Amplifier				
MS 251	0.52	100.	52.	107.
MSC 4001	1.3	25.	32.5	88.
MSC 2023-6	9.5	8.	76.	131.
Low Noise Amplifier				
AT-4641 (1st stage)	0.070	300.	21.	71.
AT-4641 (2nd stage)	0.100	300.	30.	80.
AT-4641 (3rd stage)	0.200	300.	60.	110.

[1] $\Delta T_{jmax} = \Theta_{js}$ x Dissipated Power

[2] $T_{jmax} = \Delta T_{jmax} + T_s$, where T_s is module temperature at each device location with $T_s = 55^{\circ}C$, maximum.

Table 5-20. SPACS I Breadboard Module Performance Summary

PARAMETER	REQUIREMENT	MEASURED PERFORMANCE
Transmitter		
-Frequency	2217.5-2287.5 MHz	2217.5-2287.5 MHz
-RF Output	35 dBm, min.	$\geq$ 35 dBm
-Gain	23 dB (TYP)	26 dB (TYP)
Receiver		
-Frequency	2030.9-2117.4 MHz	2030.9-2117.4 MHz
-Gain	27 dB, min.	$\geq$ 32 dB
-Noise Figure	5 dB, TYP 4.84 dB, goal 5.33 dB, max.	4.05 dB, min. 5.06 dB, max.
1 dB Gain Compression	$\geq$ 10 dBm, output	10 dBm, output (TYP) 9.45 dBm, min. 10.45 dBm, max.
T/R Duplex	Fully Duplexed	Fully Duplexed Into 1.6:1 load; IM Products $\geq$ 22 below receive carrier

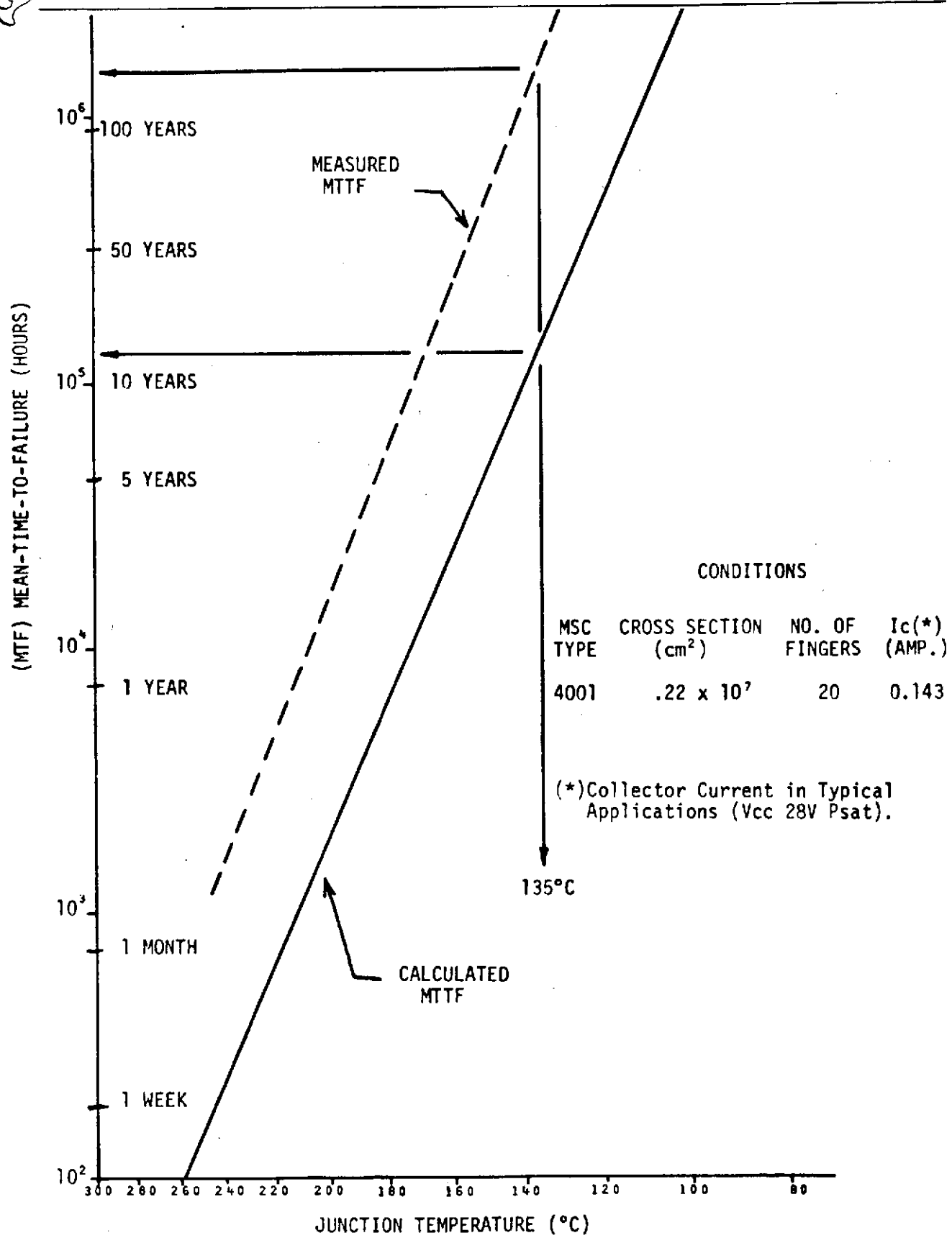
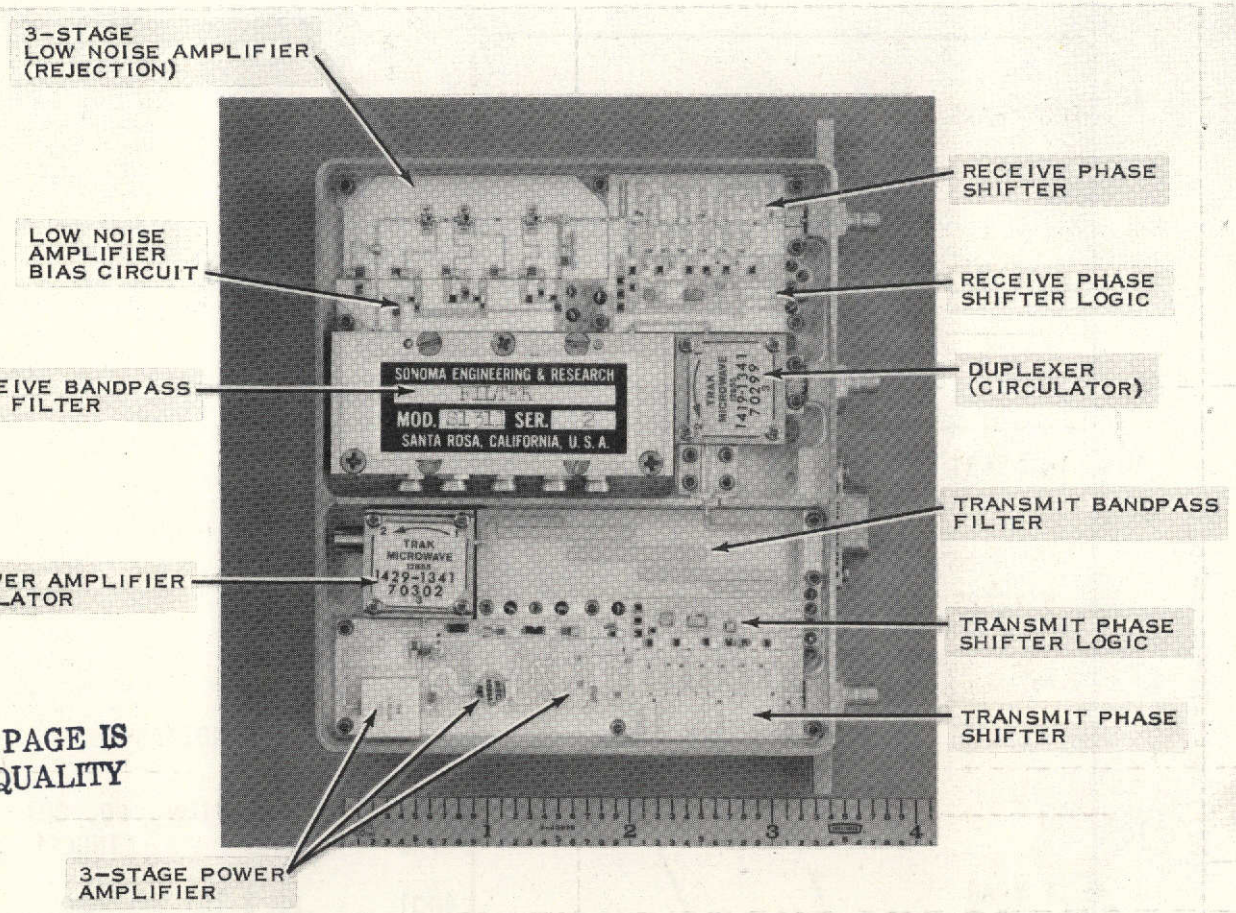


Figure 5-51. Transistor Reliability As A Function of Junction Temperature



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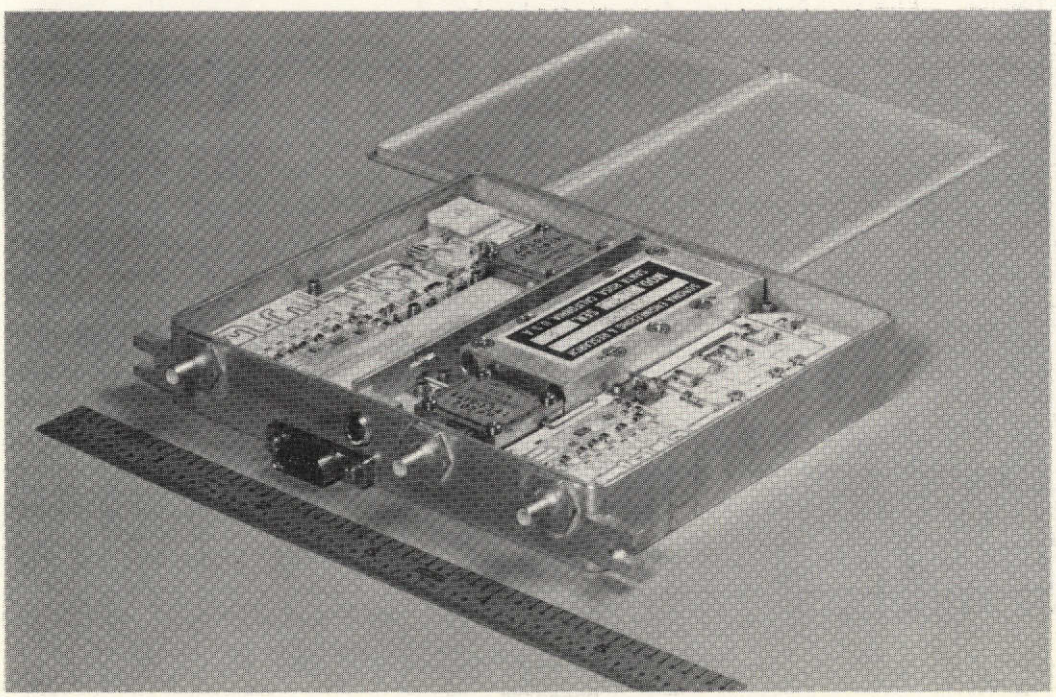

Figure 5-52. Transceiver Module, SPACS I Breadboard

- Thin-Film Microstrip Circuitry - Elimination of many components (chip resistors) and the associated labor of solder mounting these components is possible by configuring the bias and logic circuitry for thin-film nichrome resistors which would be deposited and defined during processing of the alumina networks. This approach is only cost-effective, however, for higher-volume production of these circuits. Should the module requirement extend past a design and development stage, careful evaluation of the most appropriate circuit approach should be considered.

- Isolator - Evaluation of transmitter performance without the ferrite isolator could also be considered as an approach to reduce module weight and size. Transmitter narrowband filtering provides some amount of isolation (approximately 4 dB) to antenna mismatches and might prove to be sufficient considering the present antenna element performance.

- Temperature Qualification - Further tests and design changes may be required to completely qualify the module design over the -8°C to 45°C required module case temperature range. These tests could be easily performed and the module modified slightly to meet these temperature conditions. These items would be performed on a full qualification type system design.

- Vibration Qualification - Although the module has been initially designed to meet MIL E-5400 type vibration, additional vibration tests and improvements need to be made on later contracts to fully qualify the module for NASA spacecraft type environments.

- Space Qualified Parts - The module has been designed with good quality commercial parts to meet the cost and schedule requirements under this contract. Future qualification and flight model modules would use high reliability, NASA Space approved parts.

SECTION VI

RF MANIFOLD DESIGN AND EVALUATION

A. RF MANIFOLD DESIGN

A standard balanced stripline design was used for both the transmit and receive RF manifold. Three equal (3 dB) split equal phase Wilkenson power dividers are cascaded to make an eight way power divider and combiner. One port of each manifold is terminated with a 50 Ω chip resistor to convert this design into a seven-way power divider and combiner to connect with the seven modules of the array.

The basic 3 dB power divider is shown by Figure 6-1.

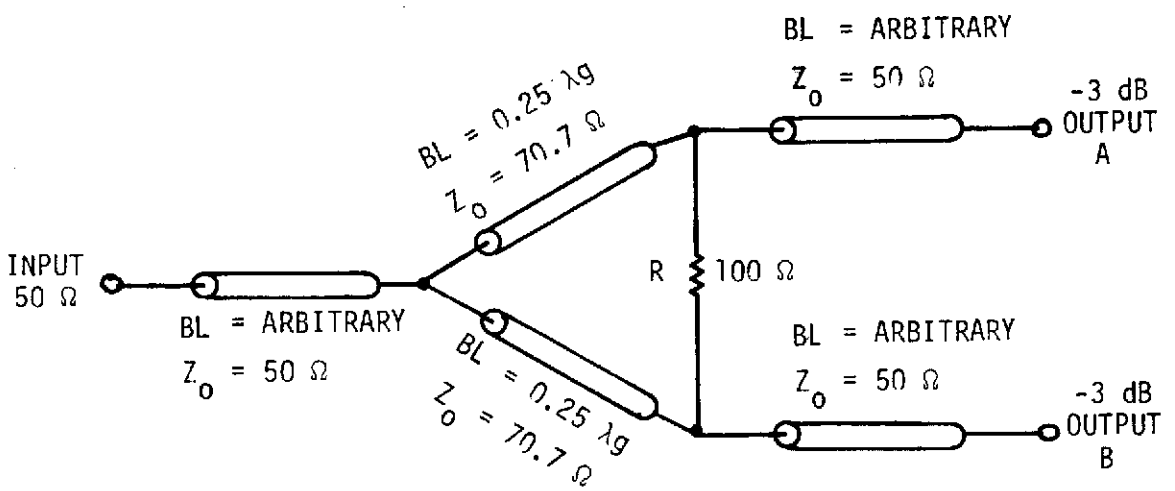

Figure 6-1. 3 dB Wilkenson Power Divider

The 100 Ω resistor used is a basic composition 1/4 watt unit.

The stripline transmission lines were laid out to have equal phase lengths for all seven ports. The RF manifolds were fabricated using 0.062 inch thick teflon - fiberglass board material for each layer. The design frequency for the transmit manifold is 2252 MHz (center frequency) and for the receive manifold is 2074 MHz (center frequency).

Pictures of the transmission line-patterns for the receive manifold and transmit manifold are shown in Figures 6-2 and 6-3 respectively. The calculated loss for each of the ports of the seven-way power dividers is:

Loss for 8-way splitter = 9.03 dB

0.25 Loss/3 dB splitter X 3 = 0.75 dB

Total 9.8 dB

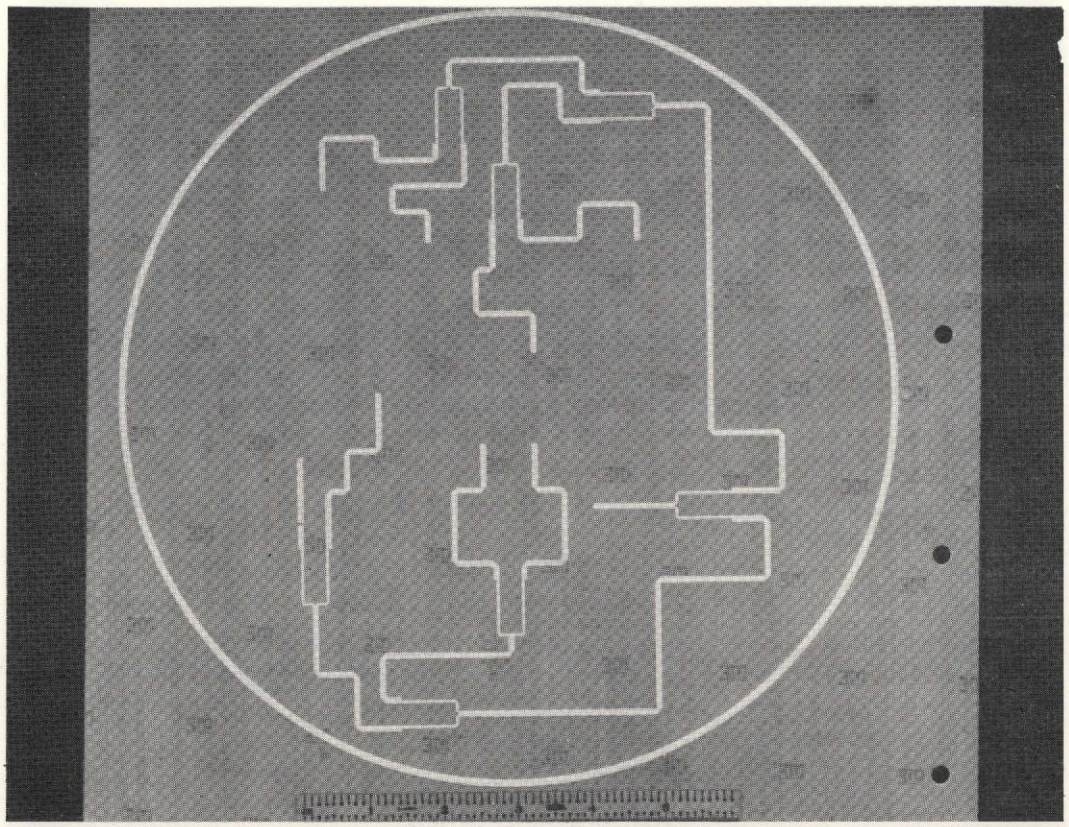

Figure 6-2. Receiver Manifold

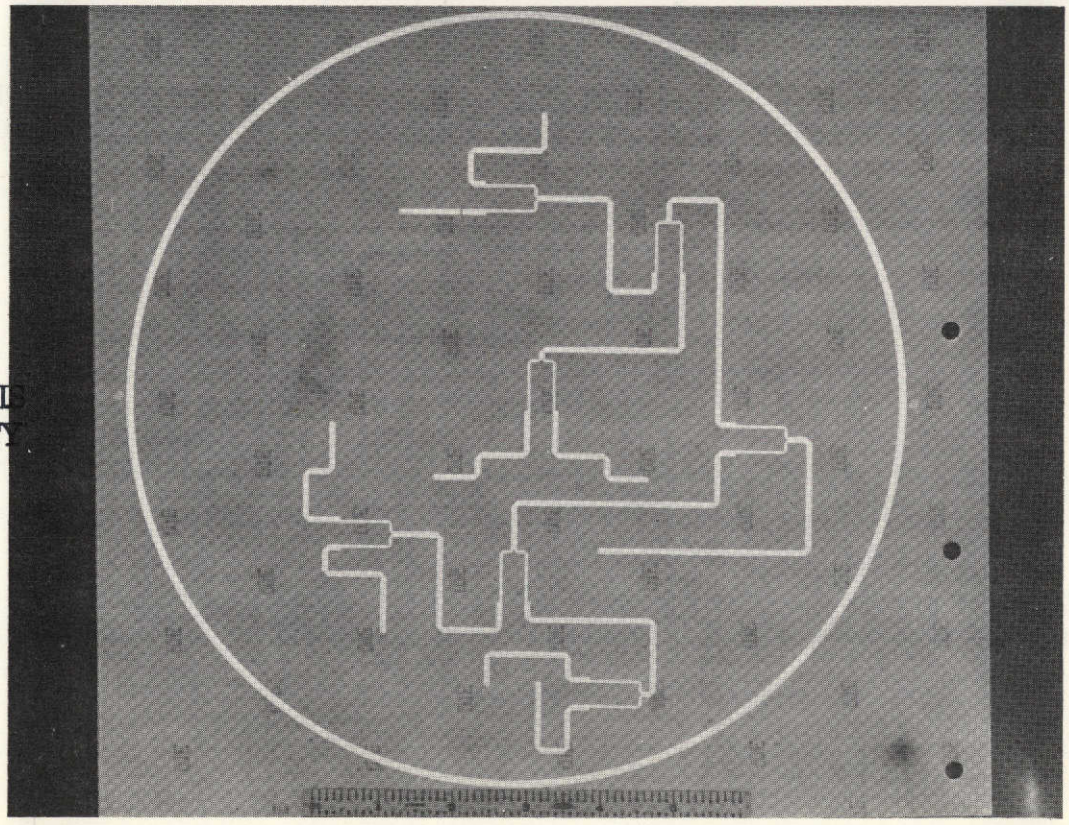

Figure 6-3. Trnasmit Manifold

Specially machined SMB connectors are mounted perpendicular through the stripline boards. Grounding ribbons are used to connect the top ground plane to the bottom ground plane of the stripline manifold. These assemblies are then clamped between support structures in the array housing.

The transmit and receive manifolds are shown clamped between typical support structures in Figures 6-4 and 6-5. The special (con-hex) SMB connectors can be seen in these photos. The transmit/receive modules have mating connectors and plug into these manifolds.

B. BREADBOARD RF MANIFOLD EVALUATION

The transmit and receive RF manifolds were evaluated by measuring them on a Hewlett-Packard Automatic Network Analyzer (ANA) model HP8542A using a Hewlett-Packard software program AGS01. One output port was measured at a time while the other six output ports were terminated with 50 Ω loads.

For these measurements both RF manifolds were clamped in place in the SPACS I array just like they would be in a final unit. A summary of this final data is shown in Tables 6-1 and 6-2.

Table 6-1. Summary of Final Transmit RF Manifold Measurements

Frequency (MHz)	Mean VSWR	Mean Insertion Loss (dB)	Mean Insertion Phase (degrees)	Phase Standard Deviation (degrees)	Mean Isolation (dB)
2210	1.26	9.53	+120.6	2.9	22.8
2220	1.21	9.54	+111.3	2.9	22.9
2250	1.09	9.56	+ 83.5	2.9	22.7
2280	1.02	9.55	+ 55.8	2.9	21.8
2290	1.02	9.59	+ 46.5	3.0	21.3

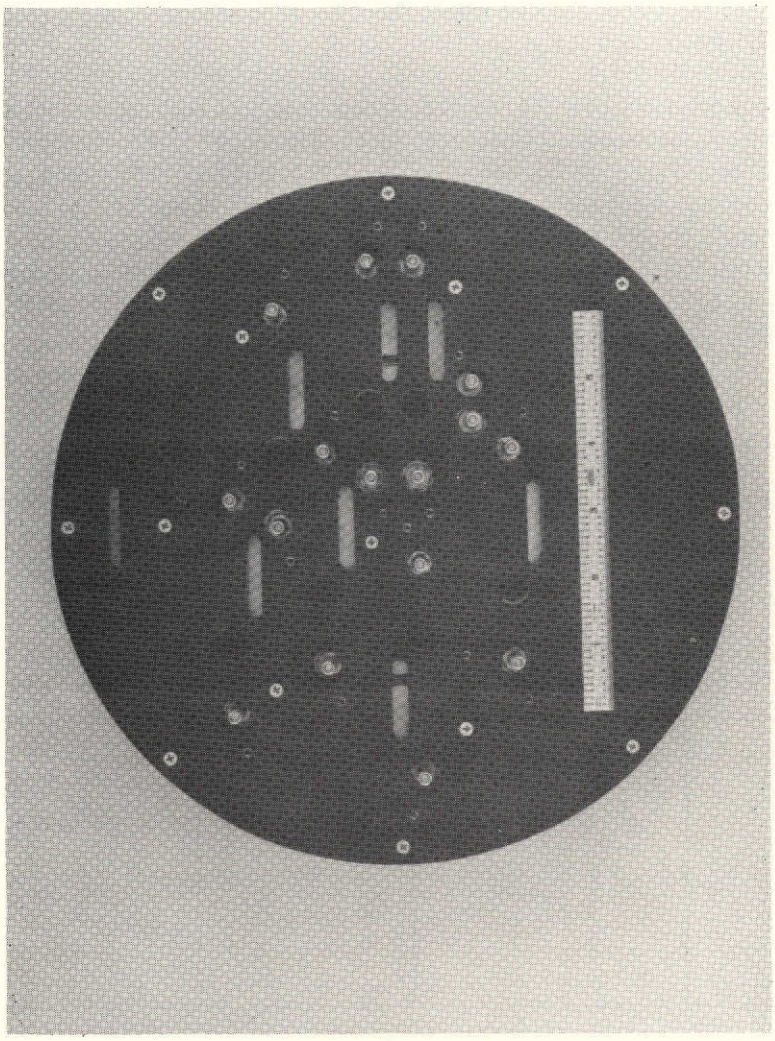

Figure 6-4. Connector Side-RF Manifold

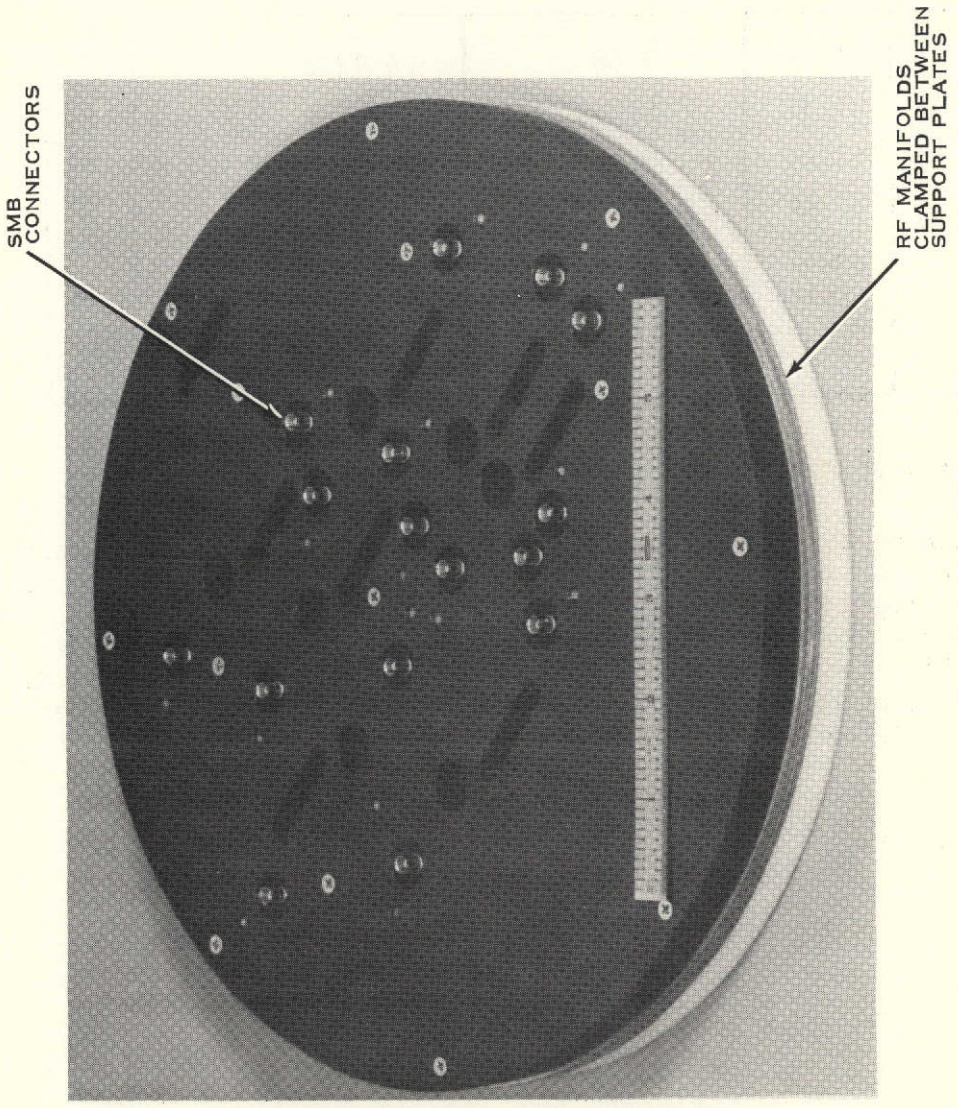

Figure 6-5. RF Manifolds (Oblique View)

Table 6-2. Summary of Final Receive RF Manifold Measurements

Frequency (MHz)	Mean VSWR	Mean Insertion Loss (dB)	Mean Insertion Phase (degrees)	Phase Standard Deviaion (degrees)	Isolation (dB)
2030	1.38	9.68	- 42.9	1.4	20.6
2040	1.31	9.68	- 52.3	1.4	21.0
2050	1.24	9.67	- 61.8	1.4	21.3
2070	1.14	9.61	- 81.3	1.4	21.8
2100	1.15	9.67	-110.0	1.5	22.4
2110	1.19	9.69	-119.6	1.5	22.4
2120	1.23	9.71	-129.2	1.5	22.5

C. SUMMARY AND IMPROVEMENTS

As can be seen from the previously summarized data, the breadboard RF manifold performance is very good. Improved performance will be obtained on future flight model RF manifolds. Improved manifolds will be of bonded stripline construction with plated through ground holes to improve electrical repeatability and uniformity. This will also reduce the affects due to different mounting and clamping techniques. With these improvements, the VSWR should be reduced and the phase difference between ports will be reduced.

SECTION VII

STEERING CONTROLLER CONCEPTS

A detailed design of the array steering controller was not performed under this contract. Too many unknowns still exist regarding the interface between the on-board computer and the antenna.

Basically each of the four arrays will have an identical phasor (logic) steering controller which will take the basic antenna scan signals and translate these into the correct phase shifter logic commands. The central power supply and controller (coordinate converter and switching unit) will interface with the aircrafts central computer to calculate the correct antenna scan signals.

To steer the transmitter beam independently of the receiver beam direction, two separate scan angle commands will be required. One of these is for the transmit angle (α_x, α_y) and one is for the receive angle (γ_x, γ_y).

These angles need to have the proper coordinate conversion to provide identical command signals referenced to the boresight of each array aperture. Thus, the appropriate coordinate transformation must be performed by the on-board computer or central controller to properly scan the lower (left and right) and upper (left and right) quad antenna array.

The antenna steering (logic) controller will consist of a single multilayer printed circuit board 8.0 inches x 3.5 inches x 0.7 inches. This circuit board will contain all the TTL integrated circuits and circuitry to perform the beam-steering functions. The board is made of etched copper circuits on epoxy fiberglass laminates that are bonded together. Where circuits must interconnect between layers or to the outside mounted active circuits, plated through holes are used. To protect the assembly, a housing of thin aluminum sheet metal will be used.

To make interconnections between this unit and the modules, a 31-pin connector will be used. This connector is of the same series as used on the T/R modules except it has more pins. The steering controller module will plug directly into a mating connector on the DC manifold. The 31-pin DC and logic connector on the steering controller will have the following pins. All logic commands will be TTL compatible signals with nominal 0 to 5 volts.

(A) Logic Input Signals

5 pins

1. Transmit pitch/yaw input data (8-bit serial word)
2. Receive pitch/yaw input data (8-bit serial word)
3. Enable Command
   +5 V array available for scan
   0 V array steered to boresight
4. Data Clock (200 nsec pulse width minimum because of minimum 200 nsec setup time, 2.5 MHz maximum PRF)
5. Module Select (7-bit serial word transmitted before data, transmit/receive pair selected together).

(B) DC Input Signals

3 pins
1. +12 volts regulated ±2% (0.35 amp)
2. Regulated Return (ground)
3. +5 volts regulated ±5% (0.92 amp)

The DC manifold will interface between the steering controller and the T/R modules. It will route the output signals correctly to the modules.

(C) Logic Output Signals to Modules

To each of six outer phasor modules.

12 pins
1. Transmitter Clock Pulse
(phasor triggers from negative going pulse edge)
2. Receiver Clock Pulse
(phasor triggers from negative going pulse edge)

Common to all six outer modules.

4 pins
3. Enable Command
4. 45° - bit command
5. 90° - bit command
6. 180° - bit command

(D) DC Output Signals to Modules

To each of seven modules.

7 pins — 1. +12 volts regulated ±2% (0.050 amp)

The +12 volt line is used to turn on and off both the transmitter and receiver in each module. By addressing the module select line, any combination of modules may be turned on or off for check-out purposes.

The center T/R module will not have phasor circuits and thus do not get logic command signals. DC signals are the only inputs required from the steering controller and DC manifold.

Basically the steering controller accepts pitch and yaw angle commands from the coordinate converter/power conditioner and calculates the six 3-bit phase words to phase the six outer module elements for the transmitter and receiver functions. In addition, the steering controller accepts a module select command which in turn turns on or off the +12 volt DC signals to the appropriate modules for module checkout.

In case of central computer failure, the coordinate converter/power conditioner would set the enable line to 0 volts (low) and switch over to an independent 1 KHz clock to drive the steering controller. These command signals would cause all the phase shifters in the modules to return to the 0° - bit positions. The array would thus be set to its on-boresight position and remain this way until the central on-board computer was restored to its normal functioning state.

SECTION VIII

THERMAL DESIGN AND ANALYSIS

A. INTRODUCTION

A preliminary study of various thermal control techniques for the SPACS I assembly has been completed. The control methods required include a combination of conduction, radiation to space, and use of circulating liquid coolants. The 112 watts of electrical power dissipated in each of the four systems must be removed from the electronics and dissipated directly to the space environment or an in-board heat sink. The orbital bondline temperature of the TPS (Thermal Protection System) covering the vehicle surface in the area immediately over the antenna ranges from -120° to 44°C for the upper quadrants and -79°C to 77°C for the lower quadrants. Allowable temperature limits for the individual module chassis are set at 0°C to 55°C. It is evident that the TPS bondline upper temperature extreme of 77°C must be reduced to achieve satisfactory electronics temperatures.

During re-entry, it will be required that only the lower quadrant mounted antennas remain operative until some time following touchdown. This means that the upper quadrant systems must only survive "storage" temperature limits during re-entry. However, the lower quadrant systems will require an in-board heat sink to "operate" satisfactorily while exposed to the transient rise of the TPS boundary to 177°C.

B. BOUNDARY TEMPERATURES

The structural support for the SPACS I consists of an aluminum bracket which is riveted to the vehicle frame. A circular carrier panel of nylon-phenolic honeycomb is also attached to this bracket to provide support for the TPS and a "window" for the antenna. Temperatures of this mounting bracket are assumed to be the same as the bondline between the TPS and the vehicle. Bondline and corresponding surface temperatures for the TPS are presented in Table 8-1 for the various operating cases.

The worst case "cold" environment occurs in the upper quadrants for a TPS bondline temperature of -120°C (-185°F). This case occurs during orbit with no direct solar heat flux incident on the vehicle surface. Similarly, the worst case "hot" environment during orbit occurs in the lower quadrants. Direct solar flux on the TPS surface results in a TPS bondline temperature of 77°C (170°F). All temperatures presented in Table 8-1 are assumed to be steady state except those presented at various points in time following start of re-entry. TPS surface and bondline temperatures are presented as a function of re-entry time in Figure 8-1. Upper quadrant bondline temperatures of 177°C (350°F) occur at approximately 1350 seconds into re-entry. Bondline temperatures in the lower quadrants remain constant at 52°C (125°F) until 1050 seconds into re-entry and then increase slowly to 82°C (180°F) at touchdown. As a result of the extremely high surface temperatures (1316°C) and large

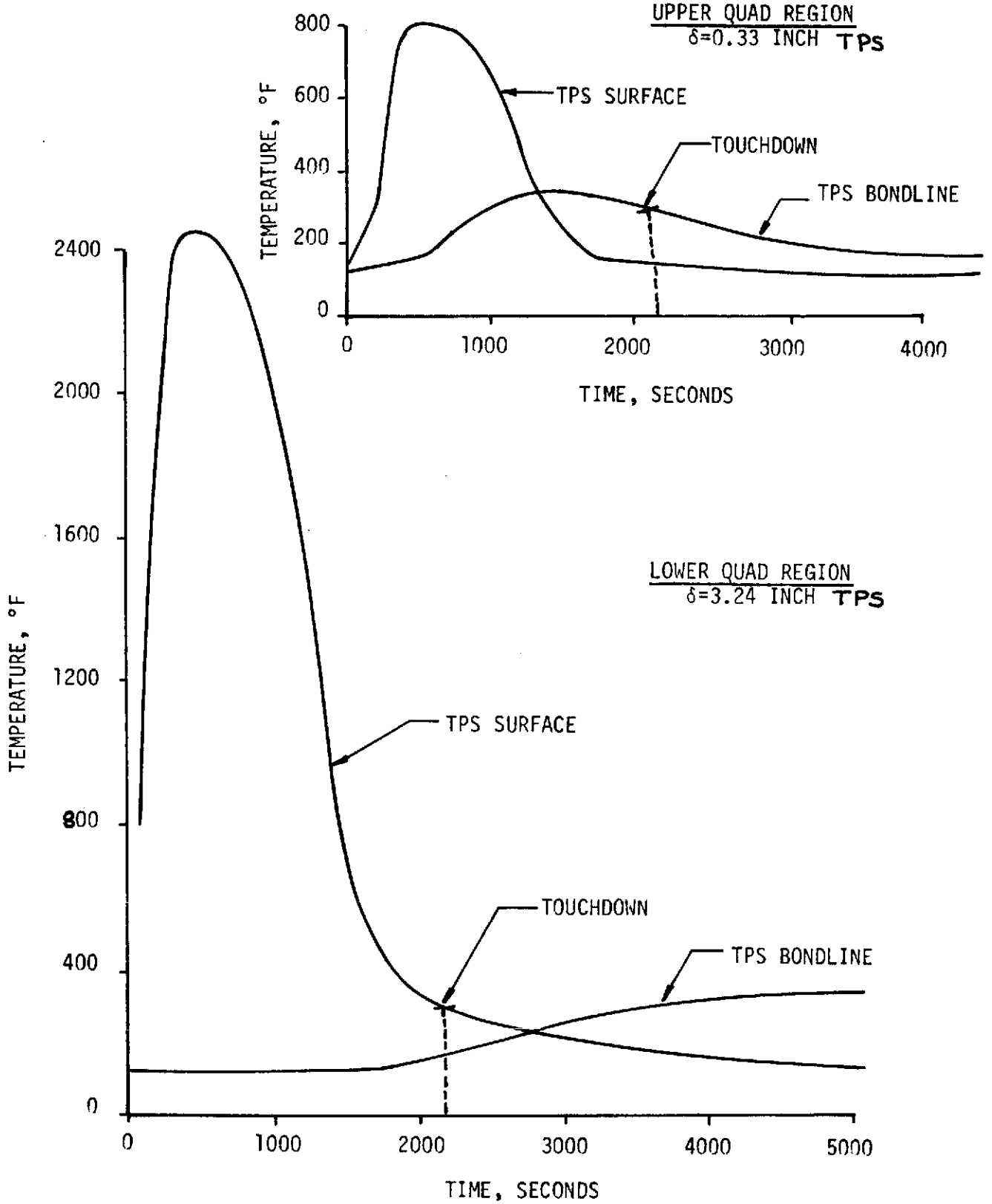

Figure 8-1. TPS Bondline and Surface Reentry Temperatures

TABLE 8-1

SPACS I BOUNDARY TEMPERATURES

			Bondline		Outer Surface	
			°C	°F	°C	°F
I.	Breadboard		35	95	35	95
II.	Pre-Launch		51.7	125	51.7	125
III.	Orbit					
	A. Upper Quads					
	1. Hot Face		44.4	112	51.7	125
	2. Cold Face		-120.5	-185	-142.8	-225
	B. Lower Quads					
	1. Hot Face		76.7	170	121.1	250
	2. Cold Face		-78.9	-110	-137.2	-215
IV.	Entry	Time, Sec				
	A. Upper Quads	0	51.7	125	51.7	125
		500	76.7	170	426.7	800
		1350	176.7	350	115.6	240
		2000	137.8	280	60.0	140
	B. Lower Quads	0	51.7	125	51.7	125
		400	51.7	125	1315.6	2400
		1050	51.7	125	982.2	1800
		2000	82.2	180	148.9	300
		5000	176.7	350	54.4	130

thermal time constant of the lower quadrant TPS, bondline temperatures continue to increase following touchdown as heat stored in the TPS is dissipated to the vehicle structure.

C. CONFIGURATIONS

The Thermal Protection System configuration in the region over the SPACS arrays has several components not used elsewhere on the vehicle. A schematic of the SPACS insulation is presented in Figure 8-2. The carrier panel is a

honeycomb structure used to support the TPS over the SPACS I array. The TPS configuration shown in Figure 8-1 for the vehicle insulation does not include the Carrier Panel or the Moisture Avoidance Pad (MAP). Thickness of the High Temperature Reusable Surface Insulation (HRSI) is 0.35-inch and 3.25-inches over the upper and lower quadrant arrays, respectively.

Thermal conductivity data versus temperature for the HRSI is presented in Table 8-2 from an orbiting temperature of -250°F to a re-entry temperature of 2300°F. The thermal conductivity values assumed for other materials in the TPS are presented in Table 8-3. There is some uncertainty as to the specific "felt" material in the Strain Isolation Pad (SIP) and the RTV material in the Moisture Avoidance Pad (MAP).

TABLE 8-2

THERMAL PROPERTIES OF HIGH TEMPERATURE
REUSABLE SURFACE INSULATION (HRSI)

T, °F	k*, Btu/hr-ft-°F	Cp, Btu/lbm-°F
-250	0.0050	0.070
-150	---	0.105
0	0.0075	0.150
250	0.0092	0.210
500	0.0125	0.252
750	0.0175	0.275
1000	0.0233	0.282
1250	0.0308	0.296
1500	0.0416	0.300
1700	0.0567	0.302
1750	0.0734	0.303
2300	0.0966	0.303

ρ_{HRSI} = 9 lbs/ft^3

* P = 0.076 torr

The composition of the SPACS I circuit board assembly is shown in Figure 8-3. There are no bond joints between any of the boards as in the TPS assembly. Honeycomb materials in the array are assumed to be the same as used in the Carrier Panel in the TPS. Further studies will be required to consider the influence of the metal inserts, fasteners, electrical connectors, and copper cladding on the temperature distribution in the circuit board assembly. Thermal conductivities for the circuit board materials are presented in Table 8-3.

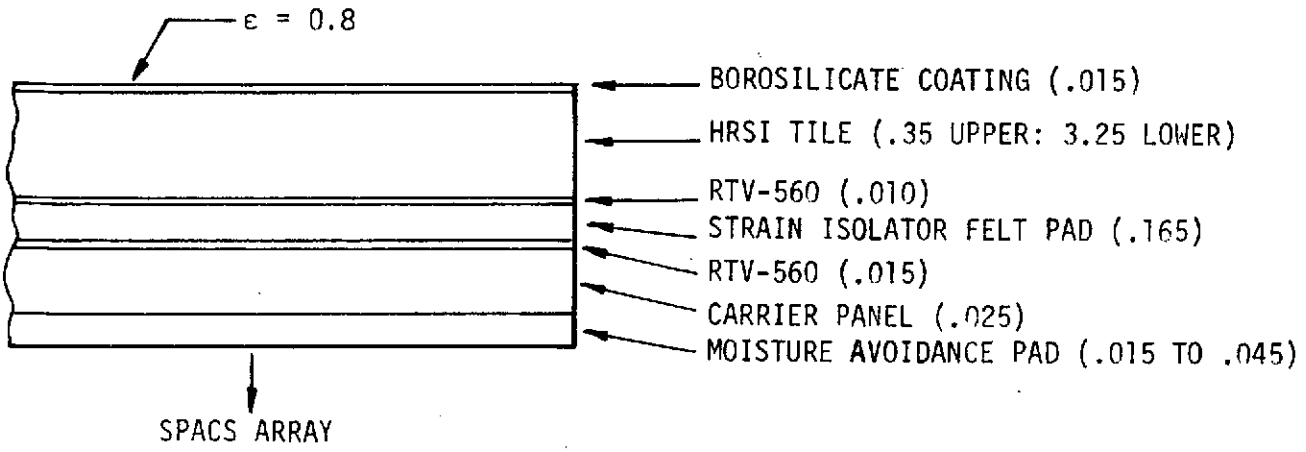

Figure 8-2. Thermal Protection System (TPS) Configuration

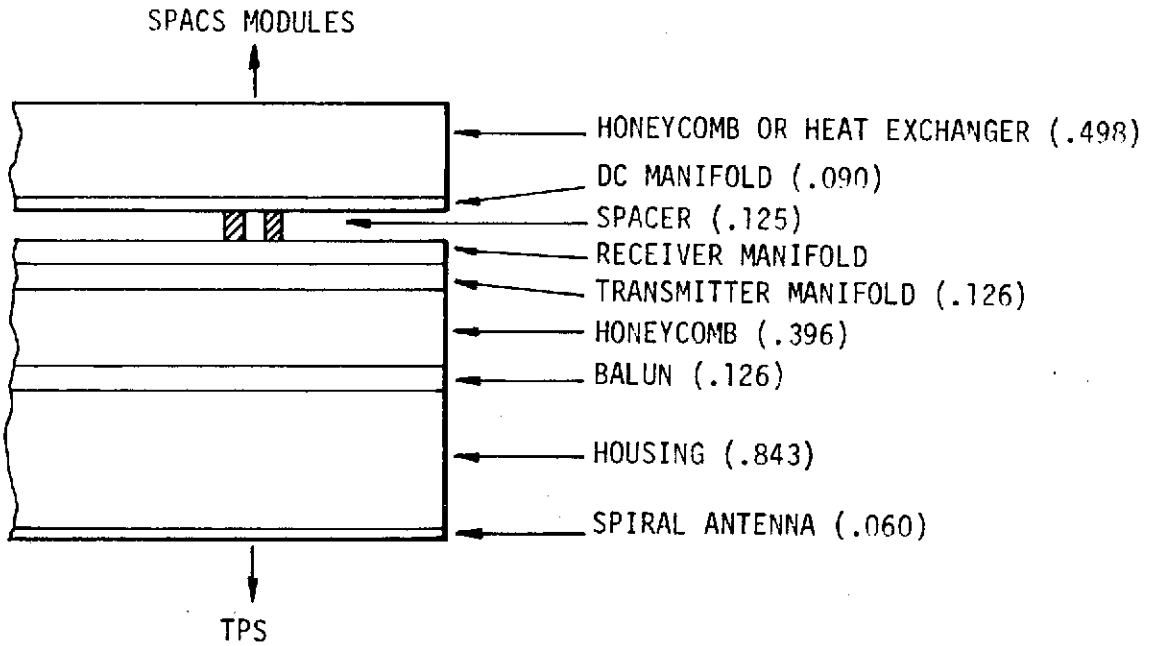

Figure 8-3. SPACS I Circuit Board Assembly Configuration

TABLE 8-3

THERMAL CONDUCTIVITY OF VARIOUS
SPACS I MATERIALS

LOCATION	MATERIAL	k, BTU/HR-FT-°F
HRSI Bondline	RTV-560	0.18
Strain Isolation Pad	Felt	0.026
Carrier Panel		0.17
Face Sheet	G-10 Epoxy Fiberglass	0.070 @ 100°F
Core	Nylon-Phenolic	0.162 @ 500°F
Moisture Avoidance Pad	RTV-560	0.18
Spiral Antenna	PTFE-Fiberglass Laminate, Copper Clad	0.063*
Balun	↓	↓
Transmitter		
Receiver		
DC Manifold	G-10 Epoxy Fiberglass Laminate	0.17

*Perpendicular to laminate.

D. THERMAL CONTROL CONCEPTS

1. TPS Radiator Heat Sink

The first method considered for thermal control of the SPACS consisted of conducting the 112 watts of dissipated electrical power through the antenna circuit boards and TPS and then radiating this power to the space environment from the TPS surface. It was assumed that the electronics are isolated from the vehicle structure with a support bracket constructed of insulating material.

The low thermal conductivity property of the LI-900 tile prohibits steady-state thermal conduction through the TPS in orbit in the same manner that it insulates the vehicle from transient re-entry heating effects. An estimate of the temperature gradiant required to conduct 112 attts across a 3.25-inch thickness of LI-900 tile having a diameter of 12.5 inches may be determined from the Fourier heat rate equation. Assuming an average tile thermal conductivity of 0.0508 Btu/hr-ft-°F from -250°F to 2300°F, the required gradient is 1310°C.

$$\Delta T = \frac{q \times L}{kA} = \frac{112 \text{ watts} \times 3.413 \times 3.25 \text{ in} \times 12}{0.0508 \frac{\text{Btu}}{\text{hr-ft-°F}} \times \frac{\pi}{4} (12.5)^2 \text{ in}^2} = 2391°F \ (1310°C)$$

A temperature gradient of this magnitude obviously is not feasible and virtually eliminates any possibility of control through the TPS

With no incident solar flux, the surface temperature of the LI-900 (emissivity = 0.8) required to radiate 112 watts to the space environment from a 12.5-inch diameter area is 296°F (147°C).

$$T_{surface} = \left(\frac{q}{\sigma A \varepsilon}\right)^{1/4} = \left[\frac{112 \text{ watts} \times 3.413 \times 144}{1.714 \times 10^{-9} \frac{\text{Btu}}{\text{hr-ft}^2\text{-°R}^4} \times \frac{\pi}{4} (12.5)^2 \times 0.8}\right]^{1/4}$$

$$= 756.3°R (296°F)$$

For the worst case "hot" mission with a nominal solar flux of 428 Btu/hr-ft^2 incident on the LI-900 tile, the equilibrium temperature of a passive, "white" thermal control surface (solar absorptance = 0.3, emittance = 0.8) is 34°C (93°F).

$$T_s = \left[\frac{428 \frac{\text{Btu}}{\text{hr-ft}^2} \times 0.3}{1.714 \times 10^{-9} \frac{\text{Btu}}{\text{hr-ft}^2\text{-°R}^4} \times 0.8}\right]^{1/4} = 553.2°R \ (93.2°F)$$

The addition of 112 watts of electrical power to the 107 watts absorbed solar energy would increase the surface temperature to approximately 202°F (94°C). These surface temperature estimates indicate that the watt density for the 12.5-inch diameter TPS surface over the antenna is much too high to achieve satisfactory electronics operating temperatures, even with special thermal control coatings.

A heat balance may be written for the TPS to determine the required surface areas to obtain satisfactory electronics temperatures. Equating the heat conducted through the LI-900 tile

$$q_{cond} = \frac{kA (T_{bondline} - T_{surface})}{L}$$

to the net heat radiated from the surface

$$q_{rad}(net) = q_{rad}(total) - q(absorbed\ solar)$$

$$= \sigma A \varepsilon T^4_{surface} - \alpha_s A \Phi_s$$

we obtain the following surface heat balance

$$\frac{kA}{L}(T_B - T_s) = \sigma A \varepsilon_{IR} T^4_s - \alpha_s A \Phi_s$$

or

$$\sigma \varepsilon_{IR} T^4_s - \frac{k}{L}(T_B - T_s) - \alpha_s \Phi_s = 0$$

where

T_s = TPS surface temperature, °R

T_B = TPS bondline temperature, °R

σ = Boltzmann constant, 1.714×10^{-9} Btu/hr-ft^2-°R^4

ε_{IR} = TPS emittance, 0.8

α_s = TPS solar absorptance, 0.3

k = LI-900 thermal conductivity, 0.0075 Btu/hr-ft-°R

L = LI-900 thickness, ft

Φ_s = Solar constant, 428 Btu/hr-ft^2

The solution to the heat balance yields TPS surface temperatures and areas required to dissipate 112 watts by radiation to the space sink. Table 8-4 contains these results for a typical TPS bondline temperature of 125°F (51.7°C), with and without incident solar flux. It does not appear to be feasible to distribute the 112 watts dissipated in the SPACE I over these large TPS bondline areas.

TABLE 8-4

REQUIRED TPS RADIATING SURFACE AREAS

Location	With Solar Flux		No Solar Flux	
	Ts,°F	A,Ft^2	Ts,°F	A,Ft^2
Upper Quads (L = 0.33-inch)	100.3	56.7	-36.6	8.7
Lower Quads (L = 3.25-inch)	94.1	446.7	-179.9	45.3

2. TPS Bondline Heat Sink

Since the SPACS I cannot be isolated from the vehicle and temperature controlled independently, the vehicle structure at the TPS bondline was considered as the primary heat sink. Bondline temperatures are presented in Table 8-1 for the various mission environments.

Maximum electronic component temperatures will be exceeded during the Mission 3A worst case "hot" environment when bondline temperatures of 77°C (170°F) occur in the lower quadrants. Junction temperatures in the MSC 2023-6 transistors would be 157°C, assuming a maximum case temperature of 77°C, 8°C/watt case-to-junction thermal resistance, and 10.0 watts power dissipation. In the actual system, there would be additional temperature gradients resulting from mounting interfaces and component heat sinks.

A finite difference thermal model of an individual, 16-watt module has been used to determine temperature gradients from the TPS bondline sink to specific components. A thermal schematic of this model is presented in Figure 8-4. The TPS, antenna circuit board assembly, module chassis, and thermal conduction paths to the TPS bondline required a total of 63 nodes. Heat generated in the modules flows through parallel conduction paths in the aluminum dust cover (nodes 59, 60, and 61) and mounting plate (nodes 15 and 61). Neglecting thermal conduction through the antenna circuit board stack, the primary thermal control path is through the aluminum housing wall (node 61 to 62) and mounting flange (node 62 to 63).

Temperature distributions in the SPACS system have been obtained for the worst case "hot" bondline temperature of 77°C (170°F). These results indicate a 52°C temperature gradient from the bondline to the MSC 2023-6 transistor case, and a corresponding junction temperature of 209°C. In order to maintain component temperatures at acceptable levels, maximum bondline temperatures and module heat sink resistances must be reduced. Increasing material thicknesses by a factor of two in the dust cover (0.062-inch), module mounting plate (0.125-inch), and housing (0.125-inch) reduces the transistor junction temperatures to 189°C. In addition to increased material thicknesses, the bondline temperature would have to be limited to 23°C (73°F) to limit component junction temperatures to 135°C as shown in Figure 8-5.

Coupling the electronics components closely to the bondline heat sink by minimizing thermal conduction resistances in the housing results in a system weight penalty and a severe heater power penalty. When the TPS bondline temperatures drop to -120.5°C (-185°F) for the worst case "cold" in the upper quadrant systems, heater power levels on the order of 18 watts per module would be required to maintain electronics chassis temperatures of -10°C. This heater power is in addition to the 16 watts electrical power per module.

A temperature profile map of the existing SPACS I breadboard is presented in Figure 8-6. This breadboard should maintain acceptable module component temperatures in laboratory test environments.

3. Self-Contained Liquid Cooling

The use of a circulating liquid coolant system between the TPS bondline and electronics modules appears to offer the best thermal control approach for minimum weight and power and a wide temperature control range. This liquid-coupled system consists of two direct transfer heat exchangers or "cold plates" coupled with a pumped heat transfer medium. One cold plate would be located in the space between the SPACS I modules and the DC manifold.

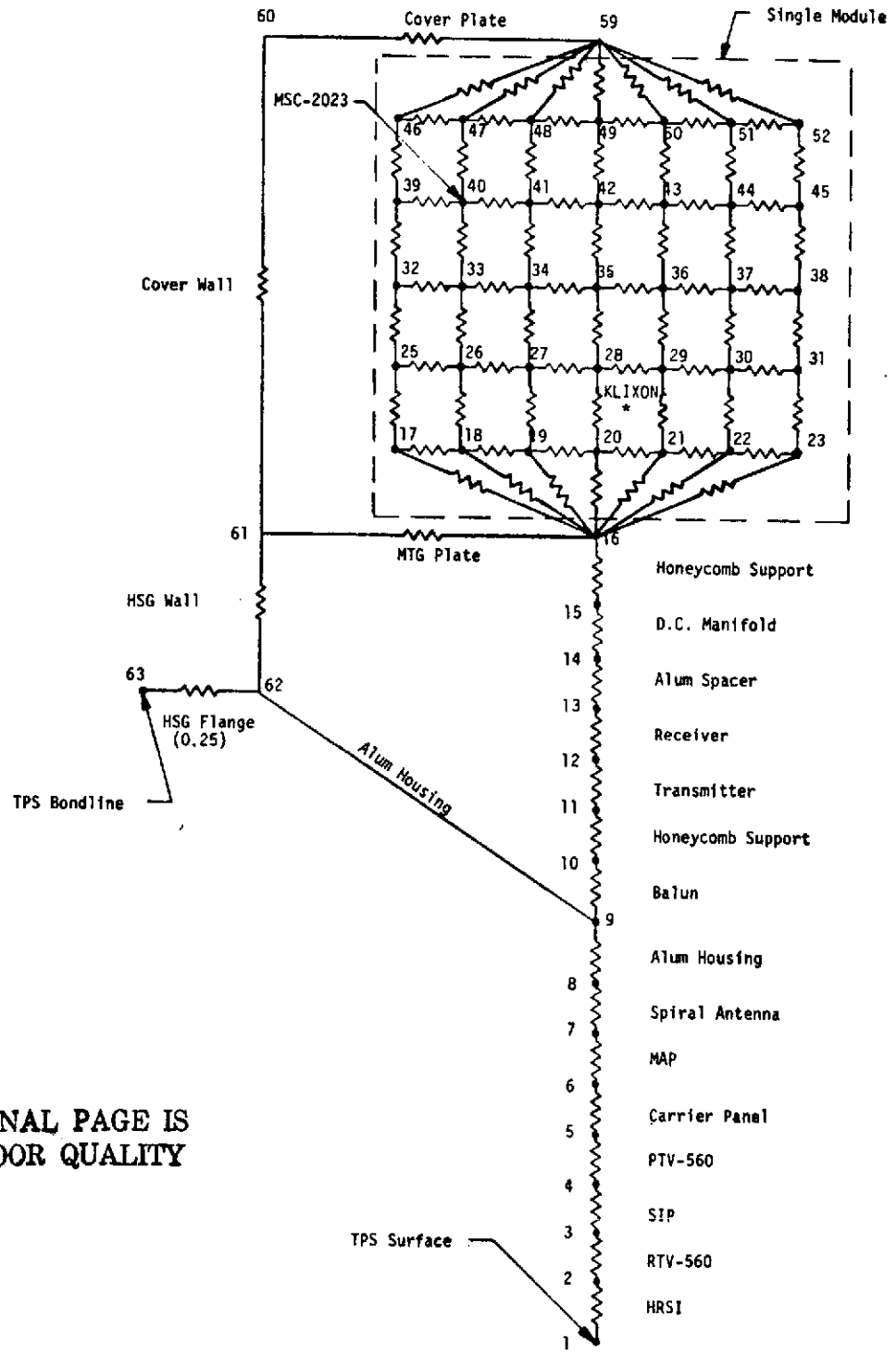

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Figure 8-4. SPACS I Thermal Model Schematic

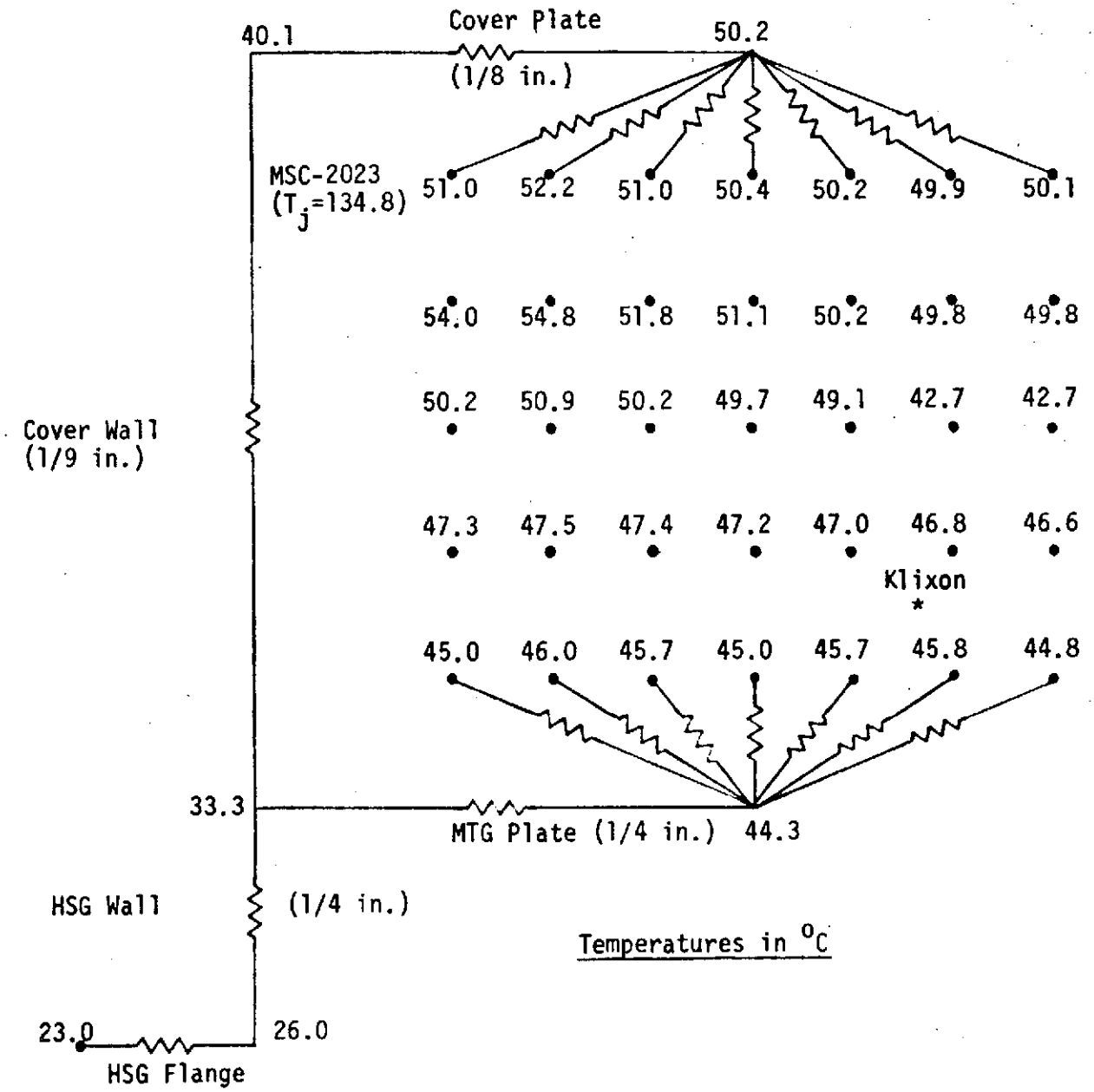


Figure 8-5 SPACS I Temperature Map For TPS Bondline Temperature of 23°C

The lower temperature "sink" cold plate would be integral with the aluminum housing between the Balun and Spiral Antenna and coupled directly to the TPS bondline. Thermal conduction coupling between the cold plates would be minimized by the large thermal resistance of the antenna circuit board stack.

A preliminary analysis has been performed to determine the feasibility of using such a liquid coolant system. Several cooling oils and a simplified heat exchanger configuration were studied to obtain estimates of coolant mass flow rate requirements and temperature gradients between the electronics and the TPS bondline. Results of this analysis indicate that heat transfer coefficients for laminar flow are acceptable. In this case, for the design of heat exchanger equipment for viscous liquids and space operation, it is necessary to use a lower unit surface conductance in order to minimize pumping power requirements.

The heat exchanger configuration assumed for this analysis is shown schematically in Figure 8-7. Each 16-watt module is cooled by the liquid flowing through a single, 4.0-inch long channel having the cross-sectional dimensions shown.

$\dot{m}$ = Fluid mass flow rate, lbm/hr

A_F = Fluid cross sectional flow area, ft

P = Channel wetted parameter, ft

Assuming a fluid mass flow rate of 1.0 lbm/min. of a 40% water--60% ethylene glycol solution at an average temperature of 51.7°C (125°F) the following terms may be determined:

P =	0.125 ft	k =	0.219 Btu/hr-ft-°F
A_F =	9.765×10^{-4} ft^2	C_p =	0.783 Btu/lbm-°F
D_h =	3.125×10^{-2} ft	ρ =	65.96 lbm/ft^3
G =	61,444 lbm/hr-ft^2	μ =	5.504 lbm/hr-ft
Re =	349	Pr =	19.7
$\overline{h}_c$ =	110.2 Btu/hr-ft-°F		

The mass flow rate of 1.0 lbm/min. results in a fluid temperature rise of

$$\Delta T = \frac{q}{\dot{m} C_p} = \frac{16 \text{ watts} \times 3.413}{60 \text{ lbm/hr} \times 0.783 \frac{\text{Btu}}{\text{lbm-°F}}} = 1.25°F$$

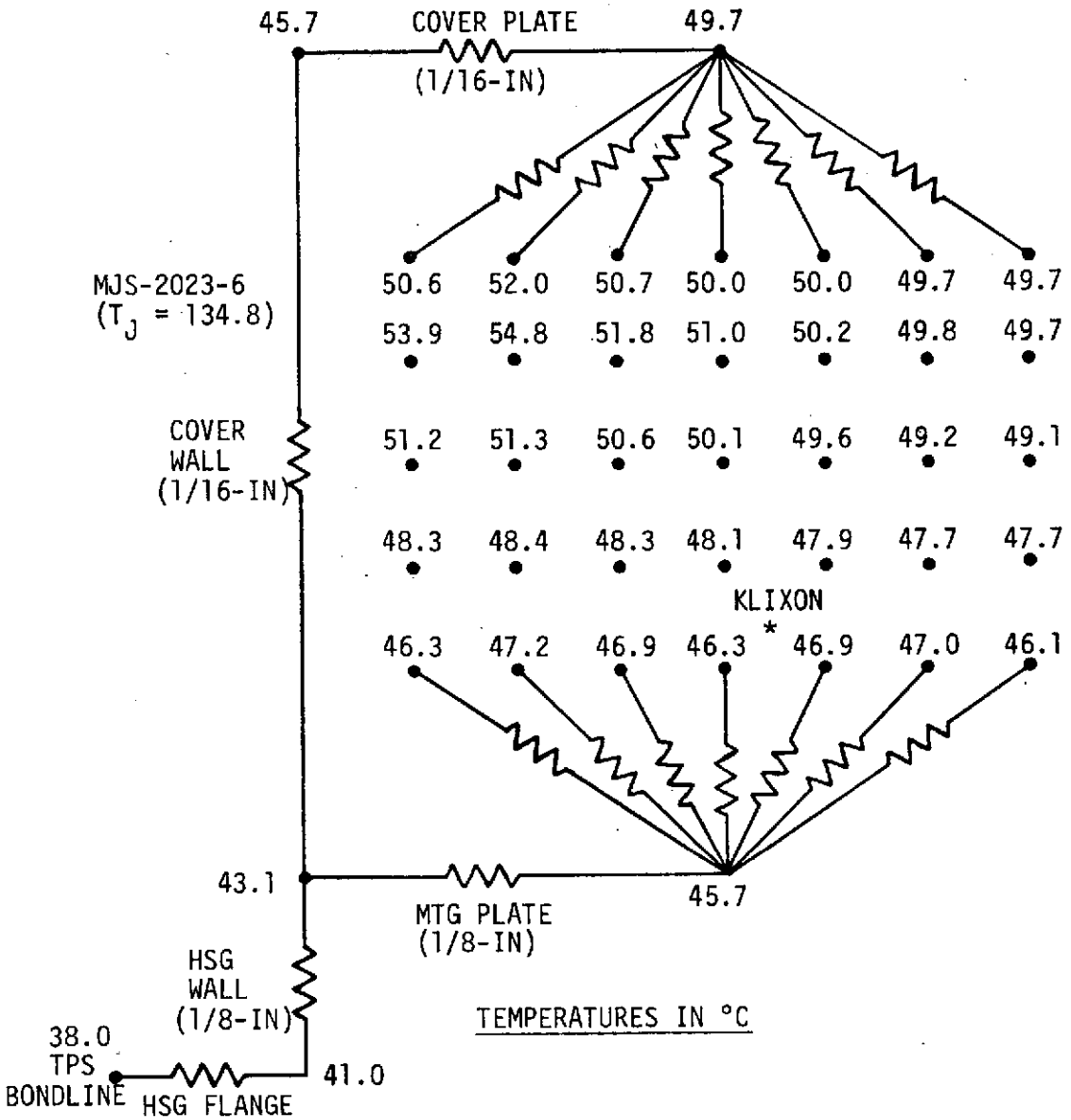


Figure 8-6. SPACS I Breadboard Temperature Map

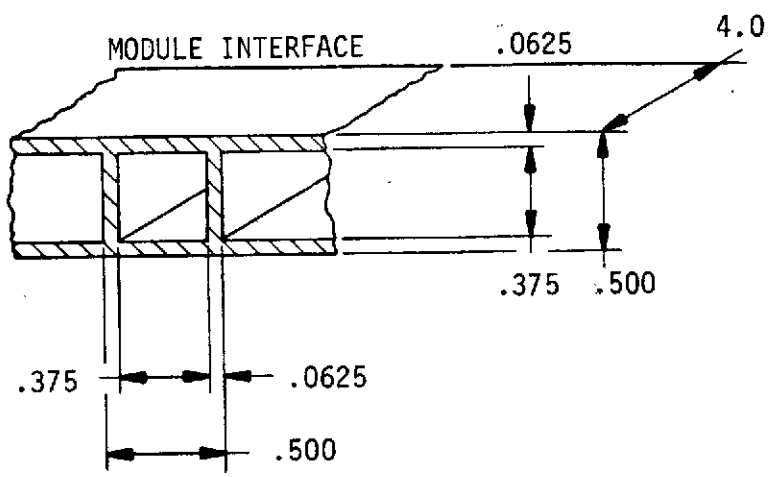


Figure 8-7. SPACS I Heat Exchanger Channel Schematic

and, an average fluid temperature of 128.1°F. The channel wall temperature is, therefore,

$$T_w = T_{fluid,avg.} + \frac{q}{R_e A_{channel}} = 128.1 + \frac{16x3.413}{110.2x.0417}$$

or,

$$T_w = 128.1°F + 11.9°F = 140°F\ (60°C)$$

Assuming the same 8.3°C channel wall temperature rise from fluid inlet for both heat exchangers, the electronics module mounting flange will operate approximately 16.6°C warmer than the TPS bondline. An additional 11°C temperature gradient to the MSC 2023-6 transistor case from the finite difference model results in junction operating temperatures of 184.6 °C for a 77°C (170°F) TPS bondline. These component junction temperatures compare closely with those for the case of increased housing material thicknesses discussed in the previous section (T_j = 189°C). The liquid cooling system has the advantage, however, of eliminating the requirement for thermostatically controlled heaters. As the TPS bondline is cooled to extremely low temperatures, the fluid flow could be continuously throttled or pumped in an ON-OFF, duty cycle mode as the cooling requirements demand.

The selection of a suitable coolant is a function of the minimum TPS bondline temperature. Freezing or pour points for various coolants range from 0°C for water to -122°C for FREON E2. As the coolant temperatures approach the freezing point, the resulting increase in dynamic viscosity of the liquid requires excessive pumping power requirements. Further analysis is required to adequately consider coolant selection, pumping system requirements, heat exchanger configurations, thermostatic controls, and vehicle interfaces.

4. Combined Self-Contained Liquid and Conduction Cooling

A solid conduction thermal link may be required to couple the SPACS I with the TPS bondline for the case of bondline temperatures below the pumping limit of the liquid coolant. The low temperature pumping limit for cooling oils such as ethylene glycol is determined primarily by the dynamic viscosity, μ, which increases rapidly as the liquid temperature approaches the pour point or freezing point. Since the TPS bondline low temperature limit is only -79°C (-110°F) in the lower quadrants, continuous pumping of a low temperature coolant such as FREON E2 (F.p. = -122°C) may eliminate the need for a solid thermal link. A schematic of the combined mode cooling system is shown in Figure 8-8. Indicated in the schematic is a transistor junction temperature range of 135°C (maximum) to 80°C for a corresponding TPS bondline range from -65°C to -120°C.

The thermal conduction link resistance of $\simeq$1.07°C/watt is determined by the minimum allowable electronics chassis temperature of 0°C, the minimum sink temperature of -120°C, and the electronics power of 112 watts. Since the antenna circuit board assembly has a large thermal resistance on the order of 165°C/watt, 16 watts maximum heater power will be required to

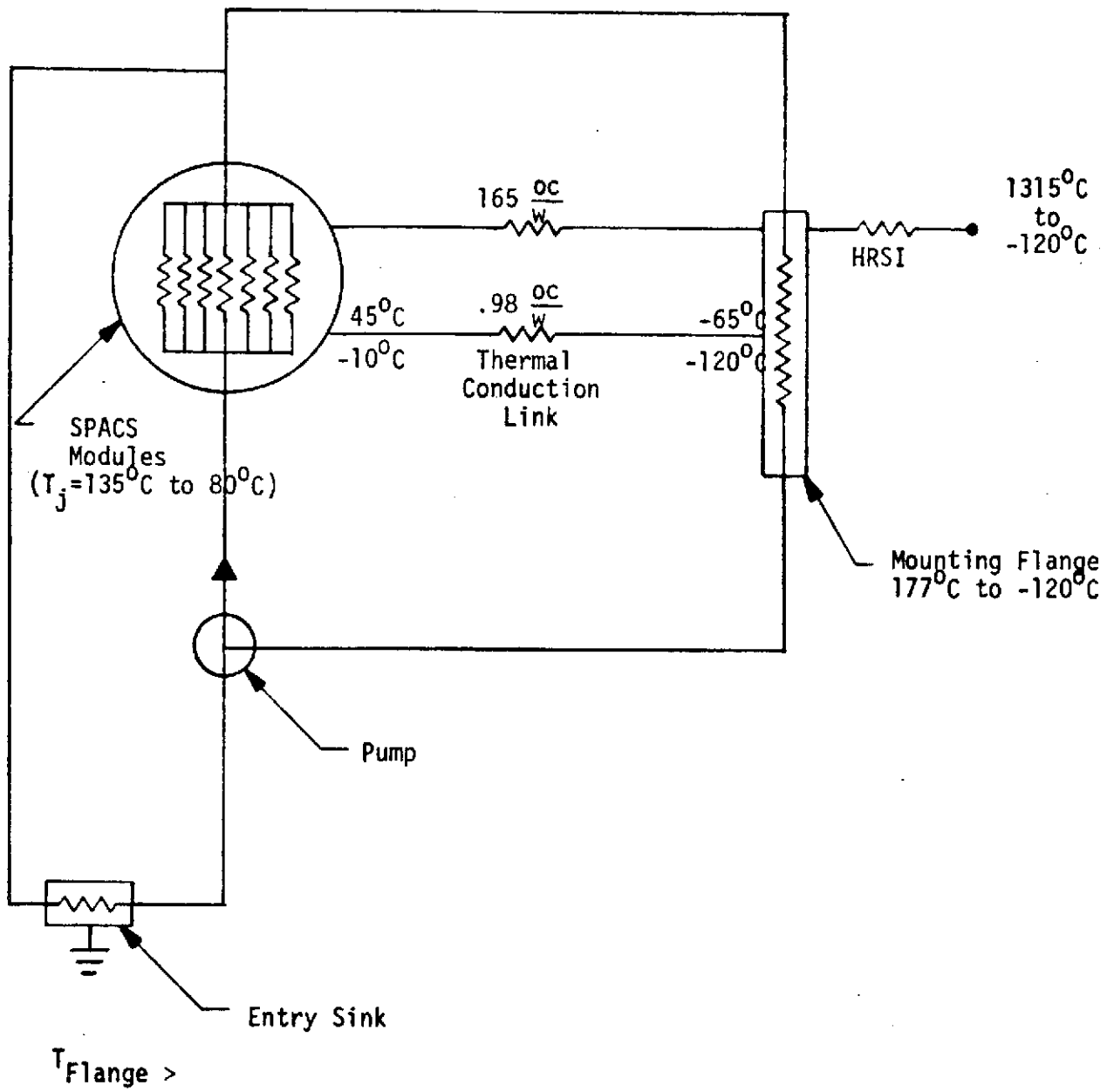


Figure 8-8 SPACS I Thermal Control Schematic

maintain 0°C electronics during non-operating periods. It is desirable to minimize the heat loss (heater power) through this thermal link during cold orbital missions and the heat gained by the SPACS I as the TPS bondline approaches 177°C (350°F) during entry.

5. Re-entry Transient

The transient response of the SPACS I to re-entry heating is a function of the conductive coupling to the TPS bondline and the feasibility of using a controlled temperature, inboard heat sink and/or liquid cooling as shown in Figure 8-7. Ideally, both systems would be coupled to the bondline with only a circulating liquid which could be shut off during re-entry. The only heating in the upper quadrants in this case would be conduction heat transfer through the antenna circuit board assembly ($R \simeq 165°C/w$) of approximately one watt, since the upper systems are non-operative during re-entry.

If thermal conduction links are required in conjunction with liquid cooling, they will result in increased electronics re-entry temperatures. This is not as severe a problem in the upper quadrant systems which must only survive storage temperature limits for electrical components and materials. However, the lower quadrant systems must operate during re-entry, as in orbit, with maximum junction temperatures of 135°C. The TPS temperatures presented in Figure 8-1 indicate initial bondline re-entry temperatures of 52°C (125°F). Although these temperatures are too high for satisfactory operation of the lower quadrant systems, the transient response from these levels may be estimated.

Assuming the electronics assembly may be approximated by a five pound lumped mass of aluminum alloy having a specific heat of 0.23 Btu/lbm-°F, a temperature rise of 0.052°C/sec will result from the 112 watts of electrical power if no active cooling is available. A total temperature rise of 104°C would occur at the end of the 2000 second entry period in the lower quadrant systems. The temperature rise of the lower quadrant TPS bondline is only 55°C from approximately 1050 seconds into re-entry to touchdown. These transients indicate that an auxiliary heat sink must be provided inboard to the vehicle to achieve acceptable electronics temperatures during re-entry in the lower quadrant arrays.

The worst case temperature rise in the upper quadrant systems may also be estimated. Assuming a thermal conduction link resistance of 1.07°C/watt and a maximum temperature gradient from 52°C (125°F) to 177°C (350°F), the electronics heat input is 117 watts. If we assume a five pound lumped mass of aluminum alloy for the upper quadrant electronics, the worst case temperature rise is 0.054°C/sec. This will result in a total temperature rise of 73°C at 1350 seconds into re-entry when the upper TPS bondline peaks at 177°C (350°F). A maximum "storage" temperature of 125°C is indicated for the non-operating, upper quadrant systems. If the upper quadrant systems are coupled to the TPS bondline with only a circulating liquid coolant, this flow might be shut off during re-entry, thus isolating the electronics.

6. Aircraft Liquid Cooling

A circulating liquid coolant system between the electronics modules and a heat exchanger located on the airframe appears to offer the only thermal control system that will meet all the boundary temperature conditions of the SPACS I array. The heat exchangers between the modules and DC manifold in all four SPACS I arrays could be coupled to a common airframe heat exchanger. Thermal conduction paths from the modules and heat exchanger to the array mounting flange would be minimized to isolate the system from temperature extremes at the TPS bondline. The high thermal resistance of the PTFE circuit boards and nylon-phenolic honeycomb support assembly would minimize heat transfer to the TPS at extreme bondline temperatures of -120°C or +177°C.

The allowable temperature range for the liquid coolant at the SPACS I heat exchanger inlet is estimated at +32°C to -8°C. This is based upon the preliminary heat exchanger analysis presented earlier for a self-contained liquid cooling system. A 7.0 lbm/min. coolant flowrate of 60 - 40 ethylene glycol-water mixture was assumed for each SPACS I array. The elimination of thermal coupling from the heat exchanger to the inboard side of the modules through the dust cover wall results in a 15°C gradient to the MSC-2023-6 transistor. This 15°C temperature gradient from the transistor case (T_{case} = 55°C maximum) to the module mounting flange in addition to an estimated 8°C gradient to the coolant results in the 32°C coolant inlet temperature upper limit. A 0°C lower limit for the electronics devices located at the module mounting flange sets the -8°C coolant lower temperature limit.

The use of an airframe heat sink for the SPACS I arrays would require extensive thermal design and analysis. Aircraft interfaces, coolant pumping and supply line requirements, and control system dynamics must be determined.

E. SUMMARY

Several thermal control concepts have been evaluated for the SPACS I electronics modules. Results of this study indicate that TPS bondline temperature extremes (-120°C to +177°C) must be reduced, or an auxiliary, temperature-controlled heat sink must be provided inboard for SPACS I electronics. This may involve coupling a liquid coolant supply from a remotely located heat exchanger. The maximum allowable heat sink temperature at each 16-watt, module mounting flange is 40°C. A brief listing of the principle results of this study are presented in the following summary.

1. TPS Radiation

Large thermal conduction resistances in the LI-900, HRSI tile prohibit transferring the 112 watts electrical power to the TPS surface. Excessive surface areas would be required at the TPS bondline to distribute this heat and obtain reasonable HRSI temperature gradients. The equilibrium temperature of a "white" thermal control coating exposed to direct solar heating is 34°C. This allows only a 21°C gradient from the radiating surface to the MSC-2023-6 transistors (T_{case} = 55°C maximum).

2. TPS Bondline

The 77°C maximum bondline temperature in the lower quadrants is excessive if the electronics are conductively coupled to the bondline. Results of a finite difference thermal model indicate a maximum bondline temperature of 23°C for a transistor junction temperature of 135°C. The low resistance conductive coupling required for the "hot" missions results in excessive heater power requirements of 18 watts per module for a bondline temperature of -120°C.

3. Liquid Cooling

A preliminary study of a circulating liquid cooling system between the TPS bondline and the electronics modules indicates a 28°C maximum allowable bondline temperature. Further study is required to select a suitable coolant for the upper and lower quadrants. Low temperature limits at the lower and upper TPS bondlines are -79°C (-110°F) and -120°C (-185°F). Liquid freezing or pour points range from -54°C (ethylene-glycol and water) to -122°C (FREON E2). The minimum temperature at which a liquid cooling system is usable is determined by the pumping power limit.

4. Solid Conduction Link

A solid conduction thermal link may be required in parallel with a liquid cooling system for thermal control below the low temperature liquid pumping limit. Selection of the optimum thermal resistance will eliminate the requirement for thermostatically controlled heaters. A 16-watt replacement heater per module would be required during non-operating periods.

5. Re-Entry Transients

Maximum temperature excursions in the non-operating, upper quadrant systems is 132°C during re-entry. Bondline temperatures in the lower quadrants are too high during re-entry for satisfactory thermal control.

Decoupling the lower electronics systems from the bondline temperature of 55°C will result in an electronics temperature rise of 104°C as a result of self-heating. Lower bondline temperatures and/or an inboard heat sink will be required for satisfactory SPACS electronics operation during re-entry.

6. Aircraft Liquid Cooling System

Coupling the SPACS I arrays to an aircraft liquid cooling system is recommended in order to meet all boundary temperature conditions. A liquid coolant temperature range from -8°C to 32°C and mass flowrate of 7.0 lbm/min. is estimated for satisfactory electronics operation. Further design and analysis is required to specify heat exchangers, coolants, pumping systems, and aircraft interfaces.

F. RECOMMENDATIONS FOR FURTHER ANALYSIS

Many problems are associated with the design of spacecraft cooling systems. In addition to passive conduction and radiation control techniques, there are fluid flow problems in the active control system required here such as pressure drop, heat transfer coefficients, fluid pumping requirements, temperature-time relations, and reliability. Only a preliminary study has been attempted here to determine the feasibility of various radiation, conduction, and forced convection cooling concepts. It is therefore recommended that the following studies be made:

- Pursue feasibility studies of passive thermal control techniques to dissipate SPACS electronics power through the Thermal Protection System (TPS)..
- Determine if TPS bondline temperature extremes are realistic for SPACS I locations.
- Study interface requirements associated with coupling the SPACS I arrays to an aircraft liquid cooling system.
- Conduct parametric studies to select suitable fluids, heat exchangers, and pumping system configurations.
- Generate a detailed three-dimensional thermal model of the SPACS I array for thermal analyzer computer program studies of temperature gradients and transients and weight optimization.
- Study fluid control system dynamics for all steady-state and transient environments and operational modes.
- Design and fabricate a SPACS I array thermal model and experimentally verify electronics temperature distributions, required fluid flowrates and boundary temperatures in a vacuum environment.
- Evaluate the use of semi-passive cooling methods for re-entry in which a heat exchanger with a boiling, expendable liquid (water, Freon 114) is used to cool a recirculating fluid.

SECTION IX

MECHANICAL DESIGN

A. MODULE MECHANICAL DESIGN

The SPACS module mechanical design incorporates proven packaging techniques for light-weight microwave integrated circuit flight hardware. The module is designed to operate in a flight and space environment and maintain device junction temperatures at or below 135°C when the thermal mounting flange is maintained between 0° to 44°C. Every effort was made to keep the module design as close as possible to an actual flight test configuration.

The mechanical module configuration shown in Figure 9-1 is 3.5 by 4.0 by 0.65 inches and weighs 0.584 pounds. The module consists of a tin-plated aluminum housing which provides mechanical support and heatsinking for the transmit and receive circuitry with associated filters and electrical switching networks. Three hermetic RF connectors, providing interface connections to the transmit and receive manifolds and the antenna array, are soldered to the module housing. One 15-pin sub-miniature DC connector provides DC power and logic distribution to hermetic feedthroughs soldered in the module housing by use of a small wiring harness as shown in Figure 9-2. In a flight hardware module this wiring harness would be replaced with a flexible printed circuit board. The module housing incorporates a divider wall as shown in Figure 9-3 to provide structural support for the cover and electrical isolation between the transmit and receive circuitry. Transmit and receive circuits are mounted to individual 0.010-inch thick nickel-clad and tin-plated molybdenum carrier plates with 63 Sn/37 Pb solder. The carrier plate subassemblies, in turn, are mounted to the module housing using miniature screws and lock washers.

The molybdenum carrier plates were chosen for the purpose of minimizing the mismatch in the coefficient of thermal expansion between the alumina ceramic circuits and the carrier plate material. This prevents excessive mechanical stresses from being transferred into the alumina and solder joints as the module is temperature cycled. Mounting the carrier plate subassemblies to the module using the miniature screws allows the carrier plate subassemblies to slide on the surface of the machined housing as the module is temperature cycled. This circuit mounting system reduces the stress levels in the alumina circuits and attachment joints below the yield strength of the materials, thus preventing overstressing of the materials during temperature cycling of the module. Also, the carrier plate subassemblies make the module easier to assemble and repair.

The module was hermetically sealed to a leak rate of less than 1×10^{-6} atm cc/second by soldering the interlocking cover to the module housing. The module cover is also of machined aluminum tin-plated construction. Final sealing of the module with an internal inert atmosphere of He/N_2 was accomplished with a seal plug as shown in Figure 9-4.

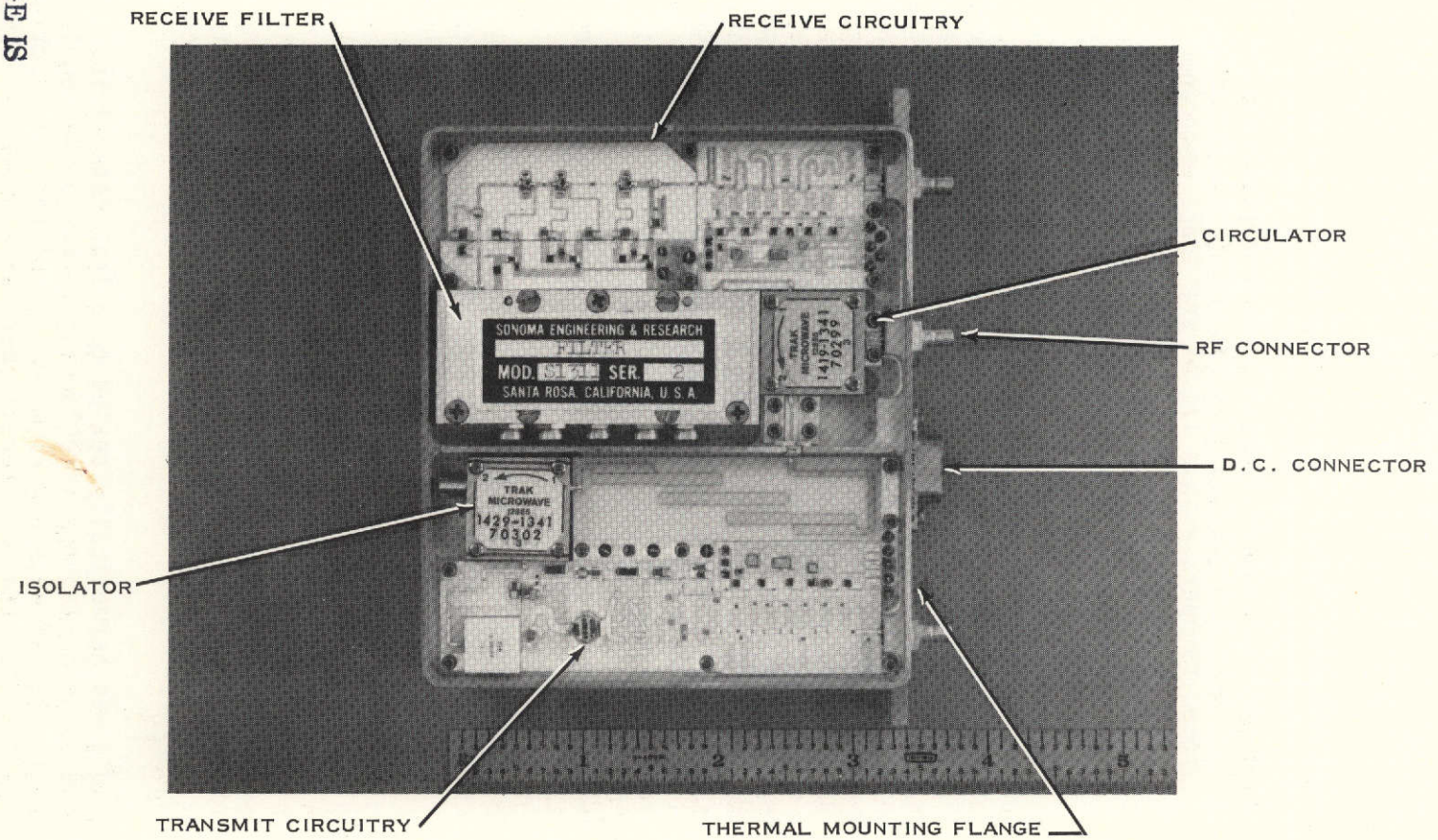


Figure 9-1. SPACS I Module Layout Configuration

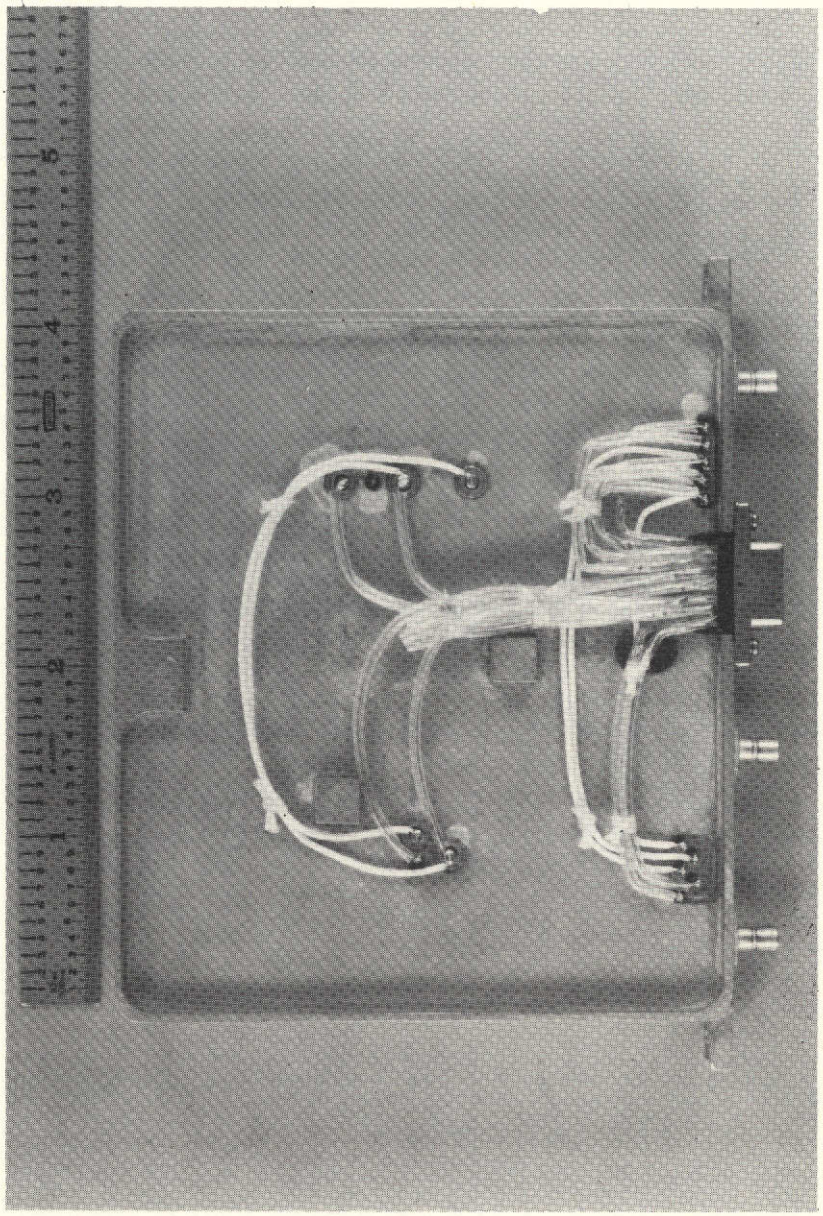


Figure 9-2. SPACS I Module D.C. Wiring View

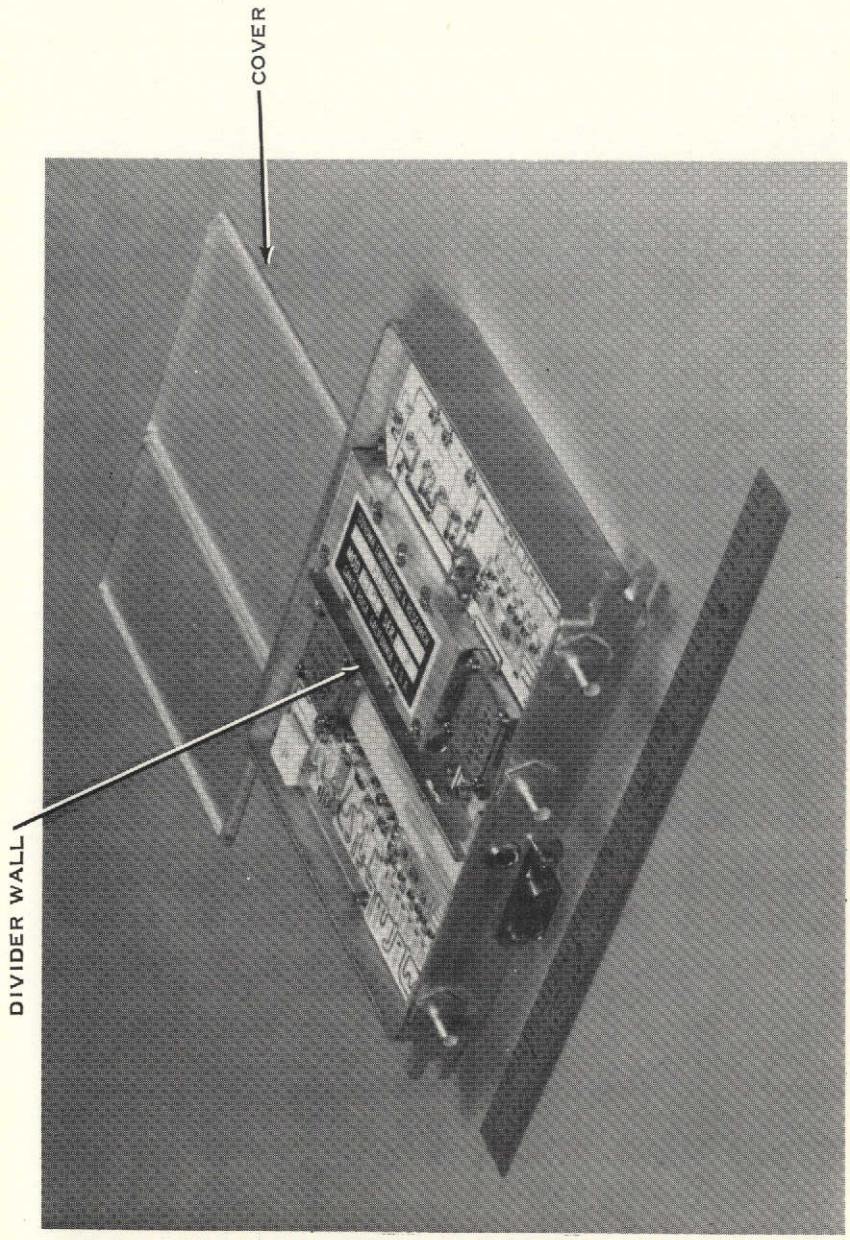


Figure 9-3. SPACS I Module and Cover

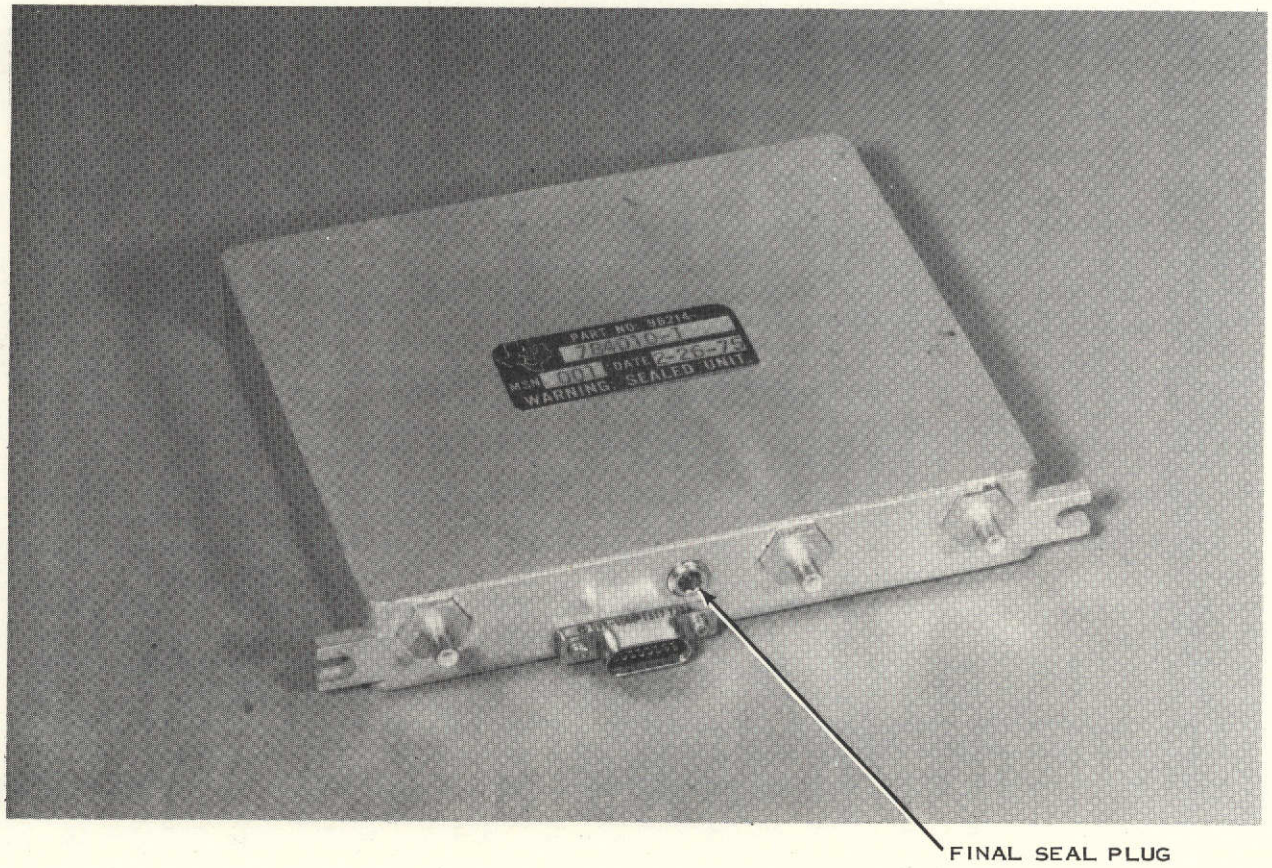


Figure 9-4. SPACS I Module

B. SPACS BREADBOARD ARRAY MECHANICAL DESIGN

The SPACS breadboard array mechanical design simulates a flight model array in as many features as could be incorporated within the hardware delivery schedule time frame. The mechanical array configuration shown in Figure 9-5 is 12.5 inches diameter by 6.0 inches thick and weighs 11.91 pounds. A detailed component weight breakdown is given in Table 9-1.

The thermal control system used in the breadboard array is as discussed in Section VIII-D-2. The main unit in this type of conduction heat transfer system is the heat conduction plate which is shown in Figure 9-6. This thermal control system will allow the breadboard array to be operated with mounting flange temperatures between -8^{0} and $+38^{0}$C.

A cross-sectional view of the breadboard array is shown in Figure 9-7. The antenna housing is a single machined aluminum structure containing the antenna element cavities, thermal mounting flange, and mounting tie points for the manifold structures, spiral antennas and heat conduction plate. The balun is a glass fluorocarbon laminate to provide electrical connection and transformation from the module to the antenna feeds and is clamped in place against the rear face of the antenna housing with an acetal plastic support structure. Mounted to the front face of the antenna housing with nylon screws is the spiral antenna circuit board containing seven (7) spiral antenna patterns terminated with high dielectric material filled epoxy. Connection between the balun and spiral antennas is accomplished by a metal tube, glass reinforced epoxy and wire twin-lead structure with solder connections at each end. The transmit and receive manifolds are glass reinforced fluorocarbon stripline structures clamped to the support structure plate with a glass manifold. Electrical connections from the module to the balun, transmit and receive manifolds are through CON-HEX SMB connectors soldered in place on the manifolds and balun. The module mounts to the heat conduction plate which is in turn secured to the antenna housing with screws. An outer cover of welded and screwed aluminum sheet metal construction provides additional module heatsinking and structural support. The outer surfaces of the breadboard array are protected with epoxy paint with the exception of the thermal interface flange.

C. SPACS I PROPOSED FLIGHT MODEL ARRAY MECHANICAL DESIGN

The SPACS I proposed flight model array mechanical design is a description of the hardware that would be built to meet all environmental conditions expected in an actual space/re-entry vehicle communciations application. The array mechanical configuration is shown in Figures 9-8 and 9-9, having an overall diameter of 12.50 inches, a thickness of 6.0 inches, and weighing 15.82 pounds. A detailed individual component weight breakdown is given in Table 9-2.

The thermal control system in the flight model array is as discussed in Section VIII-D-6. The major array thermal component in this type of aircraft liquid cooling system is the heat exchanger which is shown in Figure 9-10 and is supplied with cooling fluid with an inlet temperature of -8^{0}C to $+ 32^{0}$C. Insulating materials are used for components between the heat exchanger and

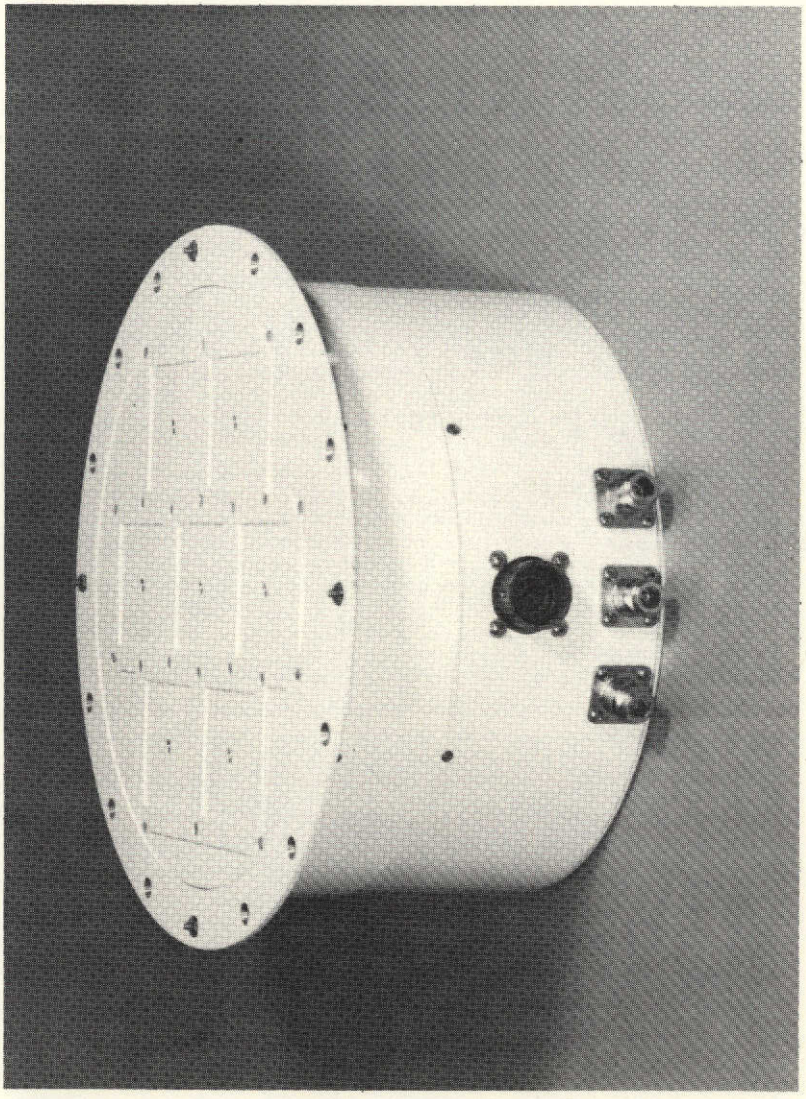


Figure 9-5. SPACS I Breadboard Array

Table. 9-1

SPACS I Breadboard Array Weight Schedule

	WEIGHT (lbs.)
Antenna Housing	3.265
Spiral Antenna	.732
Support Structure	1.357
Transmitter Manifold	.919
Receiver Manifold	.902
Balun	.900
Semi-Rigid Cables	.098
Heat Conduction Plate	1.710
Outer Cover With Connectors	1.523
Misc. And Hardware	.236
Plastic Sheet	.268
TOTAL	11.910 lbs.

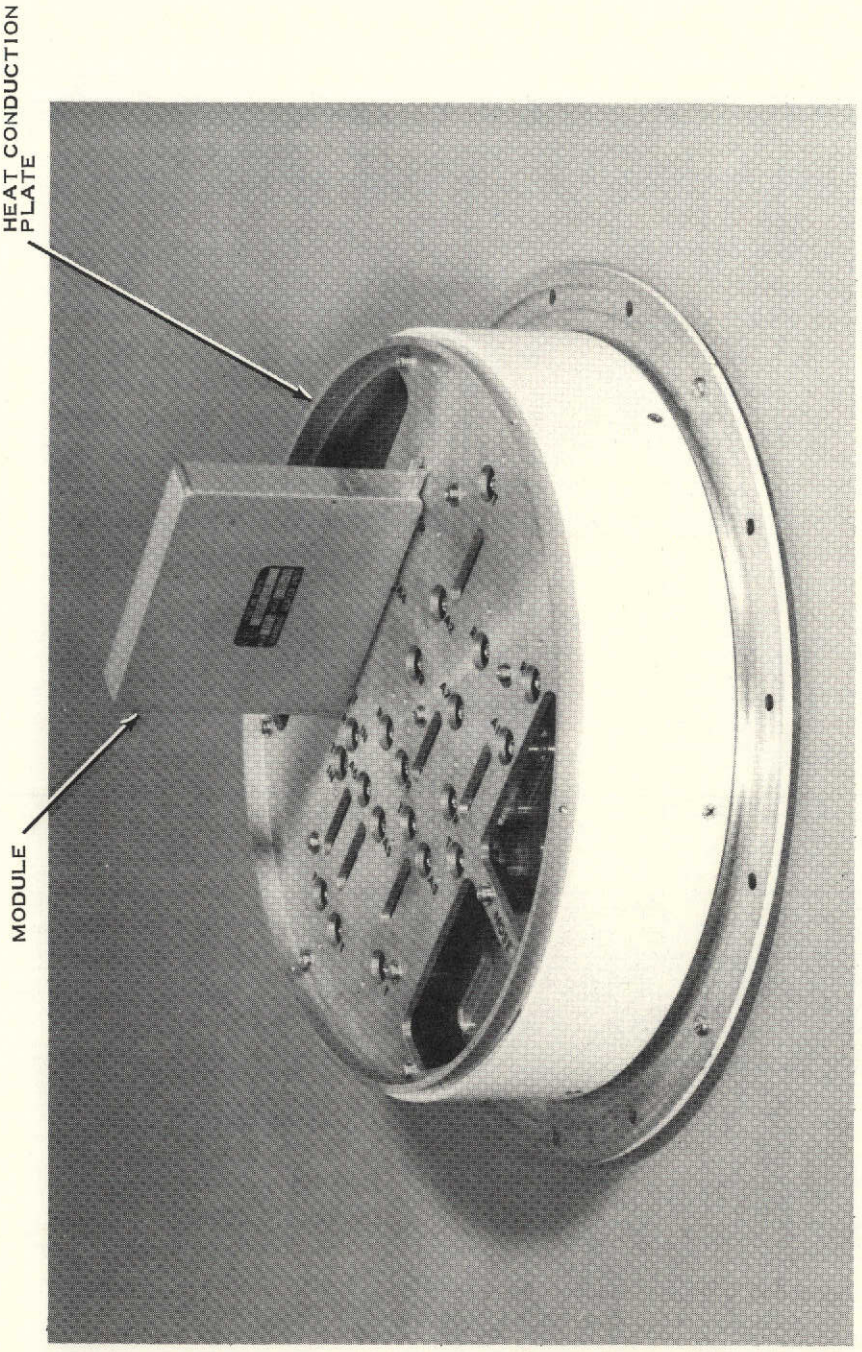


Figure 9-6. SPACS I Heat Conduction Plate With Module

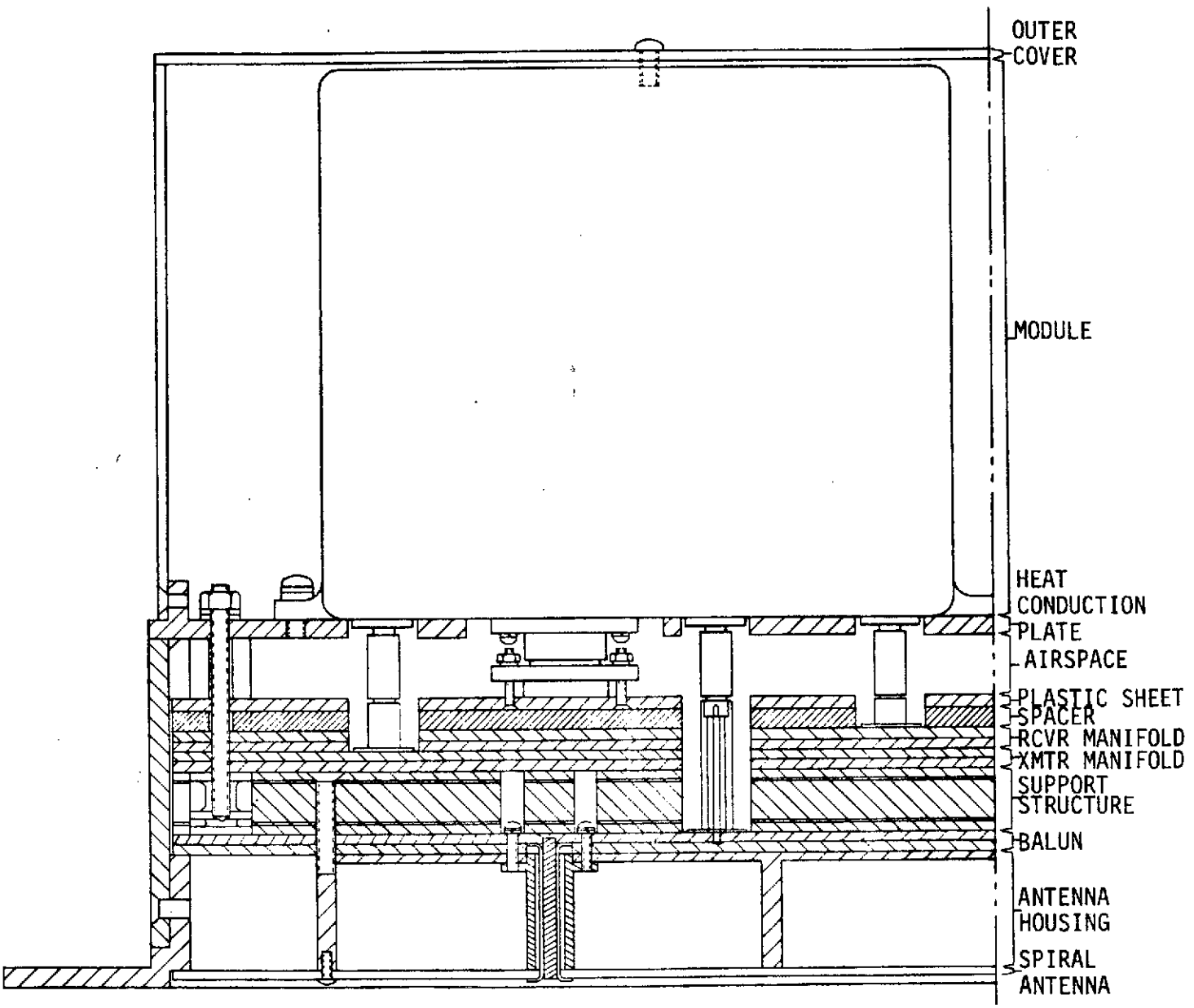


Figure 9-7. SPACS I Breadboard Array Cross-Section

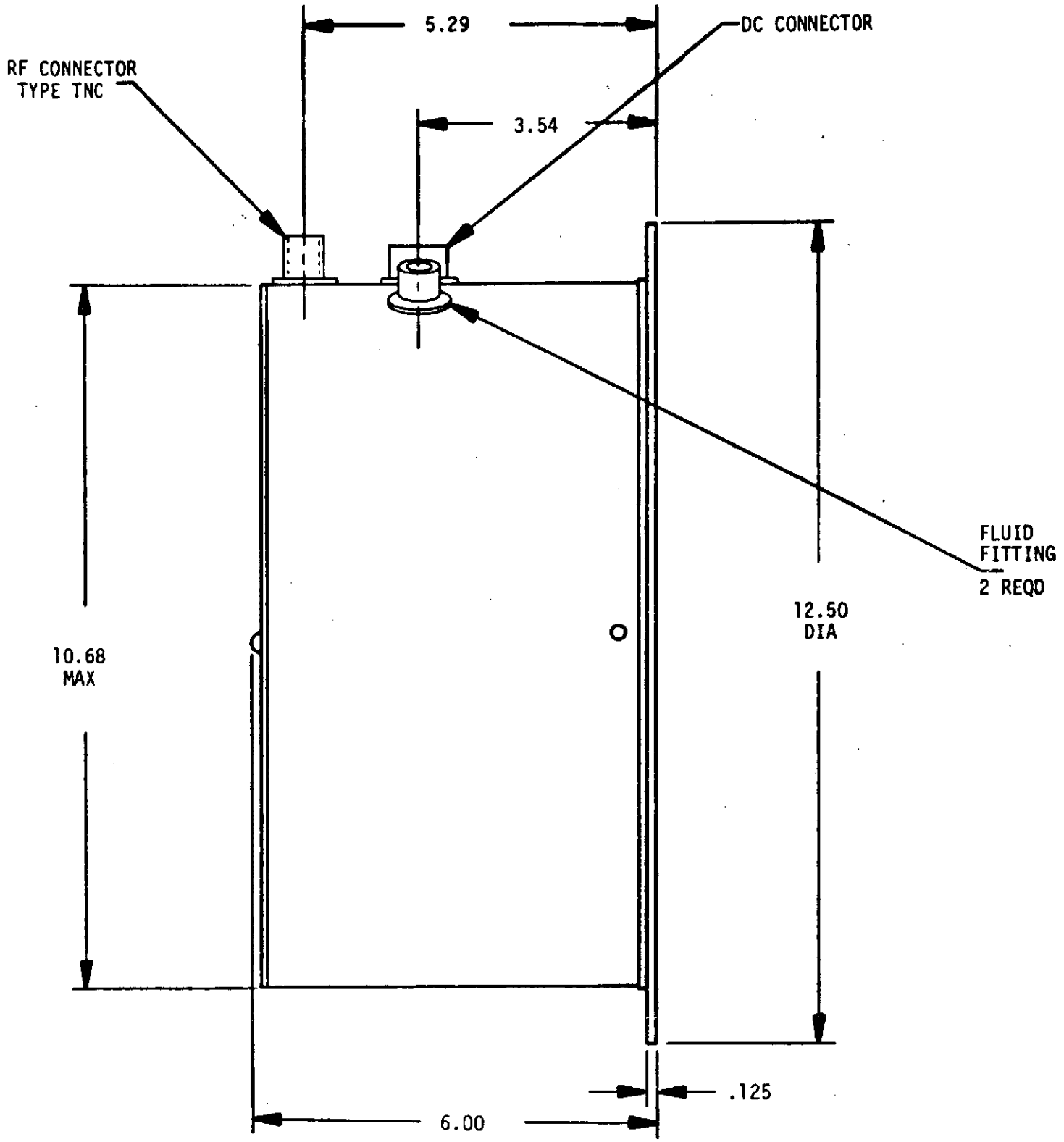


Figure 9-8. SPACS I Array - Side View

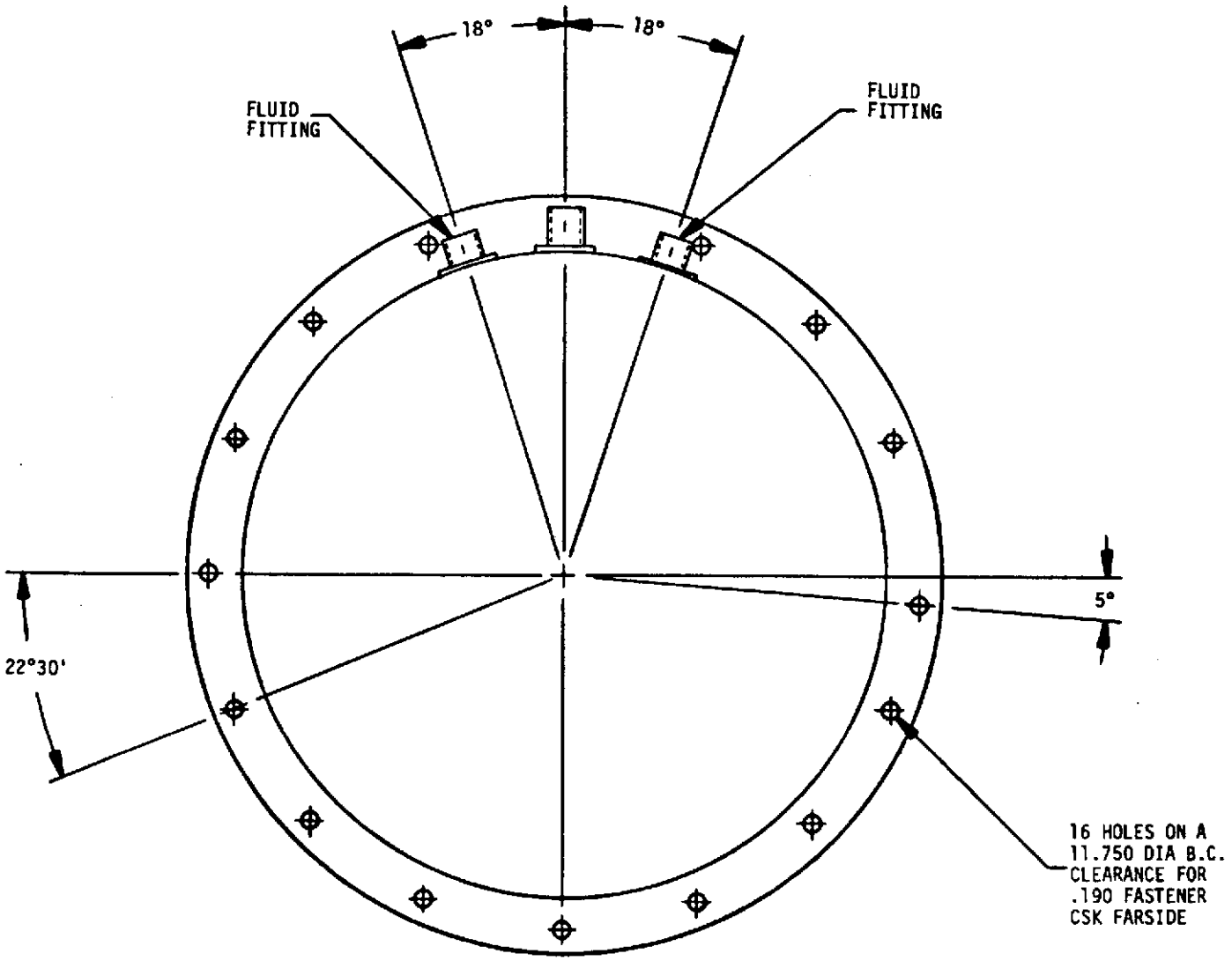


Figure 9-9. SPACS I Array - Rear View

Table. 9-2

SPACS I Flight Model Array Weight Schedule

	WEIGHT (lbs.)
Antenna Housing	1.607
Spiral Antenna	.521
Balun	.900
Honeycomb Support	.906
Transmitter Manifold	.919
Receiver Manifold	.902
Heat Exchanger	1.750
Heat Transfer Fluid	.245
7 SPACS Modules (@ .58 lb.)	4.060
Triplexer Module	.500
Steering Controller	.500
DC Manifold	.900
Wiring Harness	.660
Semi-Rigid Cables	.098
Outer Cover With Connectors	1.352
TOTAL	15.82 lbs.

the antenna housing which is mounted to the aircraft frame that has a temperature range of -120°C to +177°C.

A cross-sectional view of the flight model array is shown in Figure 9-10. The heat exchanger, honeycomb support and antenna housing are the major structural components of the design. The antenna housing is a single machined or cast aluminum structure containing the antenna element cavities, array mounting flange and various mounting locations for other array components. The balun is a glass reinforced fluorocarbon stripline board providing electrical connection and transformation from the module to the antenna feeds and is clamped in place against the rear face of the antenna housing with the honeycomb support. The honeycomb support is an epoxy bonded glass reinforced phenolic structure containing bonded-in-metal inserts for mounting screws. The spiral antenna is a double-sided glass reinforced flurocarbon circuit board with seven spiral antenna patterns on the outer surface and a ground plane, pattern to mate with the antenna housing on the inner surface. The outer turns of each spiral antenna pattern are terminated in an epoxy resistive load material and the complete spiral antenna is epoxy bonded and screwed to the antenna housing. Connection between the balun and spiral antenna is accomplished by a metal tube, glass reinforced epoxy and wire twin-lead structure with solder and/or welded joints at each end. The antenna cavity voids are filled with low-dielectric foam for mechanical support of the spiral antenna and thermal insulation of the array from the temperature extremes present at the spiral antenna/aircraft interface.

The transmit and receive manifolds are glass reinforced fluorocarbon stripline structures that are clamped and screwed to the honeycomb support. The DC manifold is a multilayer glass reinforced epoxy circuit board that is clamped and screwed to the heat exchanger. Electrical connections from the module to the balun, transmit and receive manifolds are through slide on SMB connectors soldered in place on the manifolds and balun. Electrical connection from the module to the DC manifold is through a multi-pin sub-miniature connector soldered and bonded to the DC manifold. The heat exchanger is a machined or cast aluminum structure with an epoxy bonded face plate. The modules mount to the heat exchanger which is in turn screwed to the honeycomb support with screws. An outer molded cover of glass reinforced epoxy laminate with voids filled with structural foam, provides thermal insulation and structural support to the array and modules. The exterior surfaces of the flight model array are protected with epoxy paint.

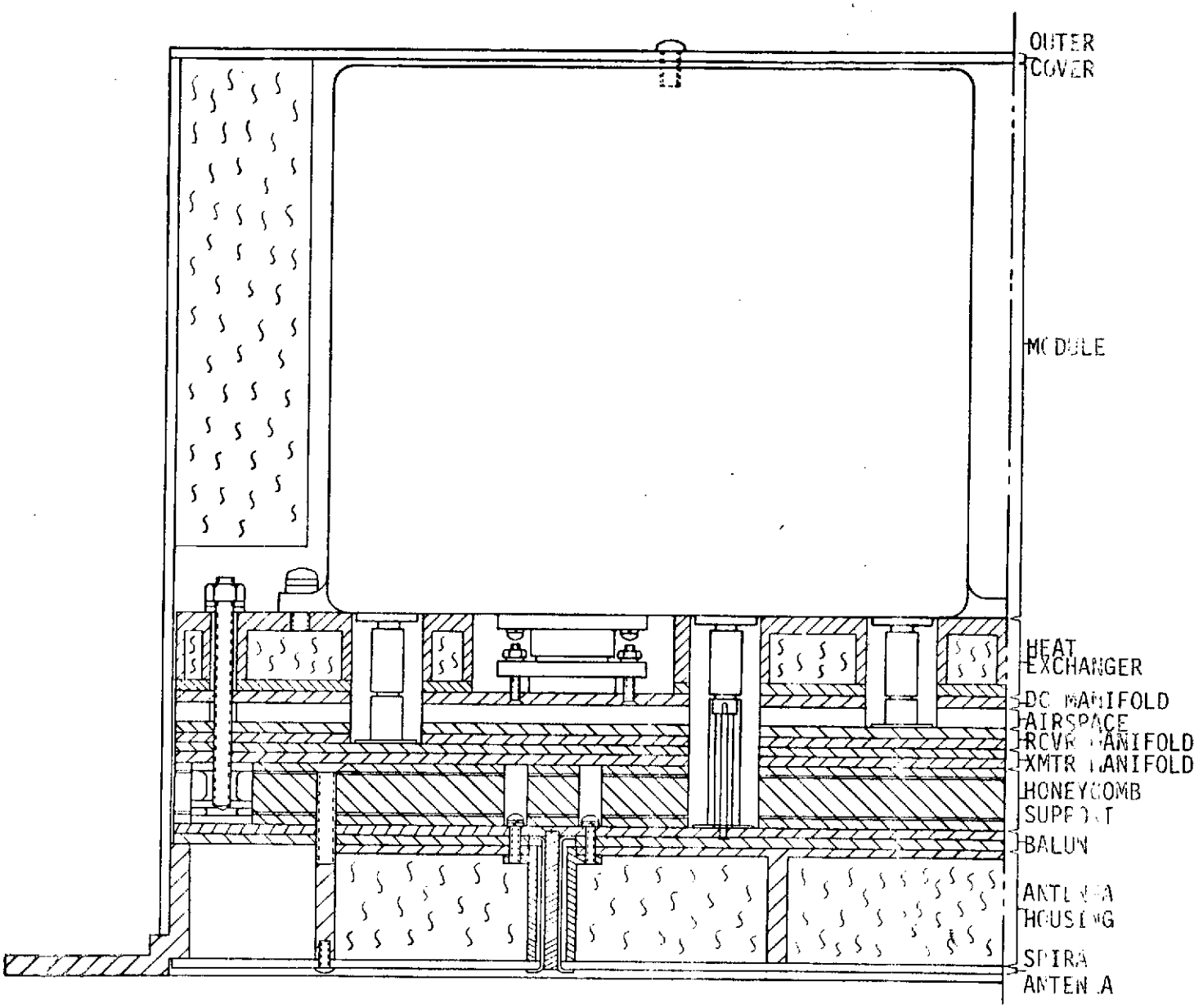


Figure 9-10. SPACS I Flight Model Cross-Section

SECTION X

COORDINATE CONVERTER AND DC POWER CONDITIONING CONCEPTS

A detailed design of the central coordinate converter and DC power conditioning equipment was not done under this contract. Too many unknowns about the central on-board computer and antenna array existed during this contract. The basic concepts of the Coordinate Converter and DC power conditioning equipment are described below.

A. CENTRAL COORDINATE CONVERTER

The central coordinate converter would receive the appropriate scan angle command from the central computer in addition to which antenna array was being selected. The coordinate converter would then perform the required rotations and transformations to reference the scan angle commands to the boresight of each array aperture. Thus each antenna array will be identical and the same steering logic command will scan each array to the same position off boresight. The coordinate converter with commands from central computer will provide the appropriate coordinate interface to drive the selected array.

The coordinate converter unit and the DC power conditioning equipment will both be located physically in the central electronics compartment of the vehicle. Shielded lines will be run for each signal from the central electronics compartment to each of the four arrays. These need to be shielded lines to keep unwanted noise and transient voltages from being picked up on these input signals. Without good shielding, array performance would be degraded.

B. DC POWER CONDITIONER

The antenna array requires 22, 12, and 5 volts regulated DC power for its amplifiers and logic functions; the power conditioner will derive these voltages from the spacecraft 28 volts DC bus. The power conditioner outputs will be DC isolated from the spacecraft DC bus so that the 5, 12, and 22 volt outputs can be grounded to the spacecraft chasis.

The DC power conditioner will consist of a transistor chopper driving a power transformer which has 5, 12, and 22 volt secondary windings. Regulation is achieved by pulse-width modulating the chopper. The power conditioner is based on a similar design used by Texas Instruments in another airborne electronics unit, and the efficiency predictions are based on this experience. The existing design uses a 15 KHz switching frequency, but switching frequencies of 10 KHz or 20 KHz could also be easily incorporated should the need arise.

On switching regulators such as this, adequate filtering is required to prevent AM and PM modulation of the RF circuitry (amplifiers and phase shifters). Especially important is to adequately (70 dB) filter the

switching frequency modulation off the DC output lines.

The DC outputs from the power conditioner to one antenna array are listed below:

a. +22 volts regulated ± 2% at 6.5 amps

b. +12 volts regulated ± 2% at 0.40 amps

c. +5 volts regulated ± 5% at 0.92 amps

d. Regulated Return (DC ground)

This is a total DC input power to one array of approximately 152 watts for the electronic circuitry in the antenna array. In addition, approximately 5 watts of DC power is required from +5 volt line for the coordinate converter. This sums up to be approximately 157 watts of power from the power conditioner.

There are three principal requirements governing the design of the power supply - a maximum available power limit of 200 watts from the spacecraft, isolation from the spacecraft power bus, and operation from an input voltage range of 25 V to 31 V from the spacecraft. Additional requirements are over-current and over-voltage protection. The isolation requirement necessitates the need for a "chopper" type supply rectifier. The input voltage variation from the spacecraft requires the need for some type of regulatory circuitry but the requirement for maximum efficiency precludes the use of a dissipative series type regulator. After many tradeoffs and power budget estimates, it was determined that the most efficient means of achieving both isolation and regulation was to incorporate the regulation circuitry within the chopper itself. This is accomplished by pulse width modulating the chopper drive in a "switching regulator" mode. A feedback loop from one of the windings in the transformer secondary provides the voltage reference for the regulator circuitry.

This type of power supply is not a new approach to Texas Instruments, and in fact, has become the standard supply in many Forward Looking Infrared (FLIR) models built by Texas Instruments. The estimated efficiency and weight budget for the DC power conditioning equipment was derived from consultation with the FLIR engineers - drawing upon their previous experience and expertise.

From these studies, the power supply efficiency is expected to be 80% overall and the weight of this equipment should be approximately 10.5 lbs. With this efficiency, the overall power required from the 28 volt ± 10% spacecraft DC bus is $\frac{157\ W}{0.8}$ = 196 watts.

SECTION XI

SUMMARY AND CONCLUSIONS

A. INTRODUCTION

This section summarizes the March 1975 status of the phased array develment work for NASA Johnson Space Center under contract number NAS9-14196 by Texas Instruments. The example array application is the Space Shuttle Orbiter. The phased array development is known by the acronym SPACS which stands for S-band phased array communication system. SPACS was developed as a research program to improve the operation of the TDRSS to orbiter link and provide data with which to compare the baseline system. If adopted it would be a part of the S-band network equipment.

The S-band communication system on the Space Shuttle is intended for communication of voice and data between the Shuttle and TDRSS (relay) satellite. A pictorial of this application is shown in Figure 11-1.

B. COMMUNICATION LINK CALCULATIONS

Based upon NASA inputs, the baseline (omni antenna array) shuttle communication link systems values were used to compare to the SPACS I parameters to determine the improvements in link performance by using a SPACS I type phased array (seven-element).

In Table 11-1 a link budget for the TDRSS-Orbiter and Orbiter-TDRSS links is shown. With the current baseline two alternatives exist.

- Operation with negative margin with resultant degradation using baseline information rates
- Operation at lower rates

The other alternative is to achieve the required carrier to noise spectral density by employing a phased array. In addition, the higher gain of the array can alleviate the need for mobile tracking stations on launch to avoid transmitting through the plume.

Shown in Table 11-2 is an abbreviated description of the SPACS performance based on SPACS I measurements. Unlike a mechanically scanned antenna, the gain of an electronically scanned antenna varies with scan. The values of the figures of merit employed, EIRP and Gain Noise Temperature Figure contain this variation and are stated as worst case values at the edge of coverage as well as at the broadside. Gains and module power outputs used in Table 11-2 were measured in February 1975 at Texas Instruments.

The steering of each array is performed at the command of the central computer. These commands are fed to the power conditioner/coordinate converter which routes steering commands to the correct array as well as DC power.

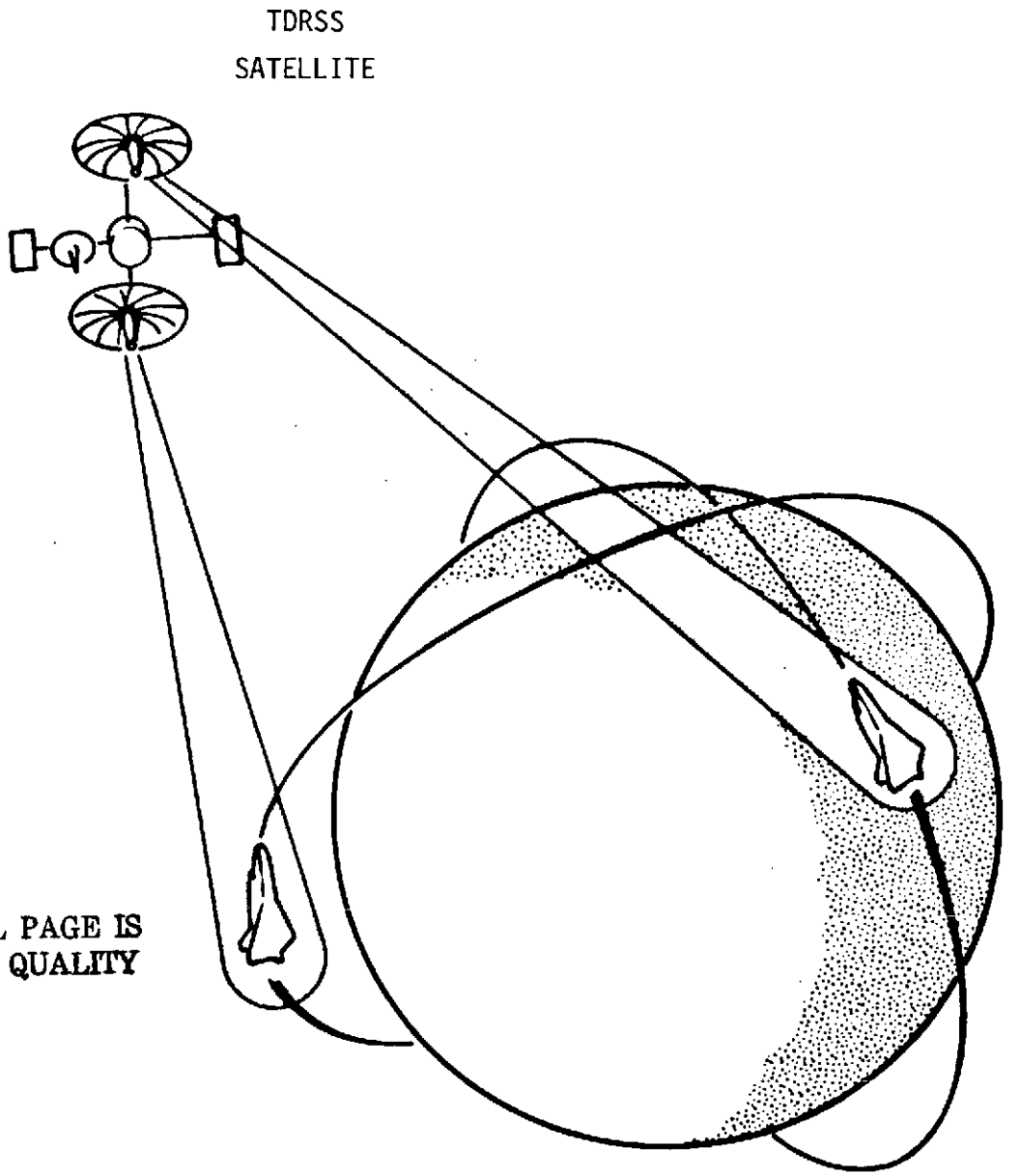


Figure 11-1. Pictorial of S-Band Communication Between NASA Space Shuttle and TDRSS Satellite

Table 11-1. Baseline (Omni Antenna) Shuttle Communications Link Calculations

TDRSS-Orbiter Normal Mode (72KBPS)	
TDRSS EIRP (dBW)	47.0
Transmission Losses (dB)	-191.9
Receive Antenna Gain (dB)	3.0
Receive Circuit Loss (dB)	- 4.9
Signal Power @ Receiver (dBW)	-146.8
Noise Temperature (dB°K)	27.1
Boltzmann's Constant (dBW/°KHz)	-201.5
C/No (dB-Hz)	54.7
Bit Rate (dB-Hz)	48.6
S/N (dB)	6.1
Eb/No For BER 10^{-4} (dB)	8.4
Coding Gain (dB)	4.5
Misc. Losses (dB)	- 3.5
Required Eb/No (dB)	7.4
Margin (dB)	- 1.3

Note: Voice Mode Margin 0.3 dB,
Low Rate Mode Margin 1.6 dB
Space Loss Calculated at 2106.4 MHz
and 22,786 Nmi

Orbiter-TDRSS Normal Mode (192KBPS)	
Orbiter Transmitter Power (dBW)	20.5
Orbiter Transmit Circuit Losses (dB)	- 7.5
Orbiter Antenna Gain (dB)	3.0
Orbiter EIRP (dBW)	16.0
Transmission Losses	-193.1
TDRSS Antenna Gain	36.0
Signal Power @ Receiver (dBW)	-141.1
C/No dB-Hz	59.8
Bit Rate (dB-Hz)	52.8
S/N (dB)	7.0
Eb/No For BER 10^{-4} (dB)	8.4
Coding Gain (dB)	4.5
Misc. Losses (dB)	- 3.5
Required Eb/No (dB)	7.4
Margin (dB)	- 0.4

Note: Low Rate Mode Margin 2.6 dB,
Space Loss Calculated at 2287.5 MHz
and 22,786 Nmi

Baseline System

(Worst Case Analysis)

Table 11-2. Summary of SPACS I System Performance

7 Element S-Band Antennas Spaced at 90° Intervals About The Spacecraft (Four)

- Minimum EIRP over a 100 X 140 cone is 19.5 dBw
- Maximum EIRP at broadside is 25.5 dBw
- Input power level 30 dBm at switch input (1 watt)
- Minimum gain/noise temperature over a 100 X 140 cone is -21.7 dB/°K
- Maximum gain/noise temperature at broadside is -15.7 dB/°K
- Receive electronic gain 25 dB
- DC power 196 watts (22-30 volts)
- Weight 16.0 pounds each array (four arrays)
- Transmit frequencies 2217.5 and 2287.5 MHz
- Receive frequencies 2041.9, 2106.4 MHz
  1775.9, 1831.8 MHz
- Dimensions 10.68" diameter X 6" height

Power Conditioner/Coordinate Converter

- Provides conditioned DC voltages to each array
- Converts pointing angles for the system into array angles for correct phasing of modules

S-BAND PHASED ARRAY COMMUNICATION SYSTEM (SPACS I)

The comparison between SPACS and the baseline system is summarized below for the normal worst case mode.

	BASELINE MARGIN	SPACS MARGIN
TDRSS-TO-ORBITER	-1.3 dB	9 dB
ORBITER-TO-TDRSS	-0.4 dB	3.1 dB

The S-band subsystem consists of four arrays located as shown on the orbiter in Figure 11-2. The SPACS I arrays would replace the omni antennas which are currently located here. Structural provision has already been made to accommodate a larger antenna into the vehicle skin. Provision for cables to control the pointing of the array has also been accomplished.

A block diagram of the conventional baseline S-band equipment is shown at lower left of Figure 11-2. Each array is a one for one replacement for the four leftmost omni antennas. If SPACS I were employed the preamplifier and power amplifier would be deleted from this diagram and replaced by an assembly which supplies each antenna with conditioning and logic circuitry which directs the antennas beams. A diplexer is also contained in the replacement assembly since this function is currently performed in the pre-amplifier assembly.

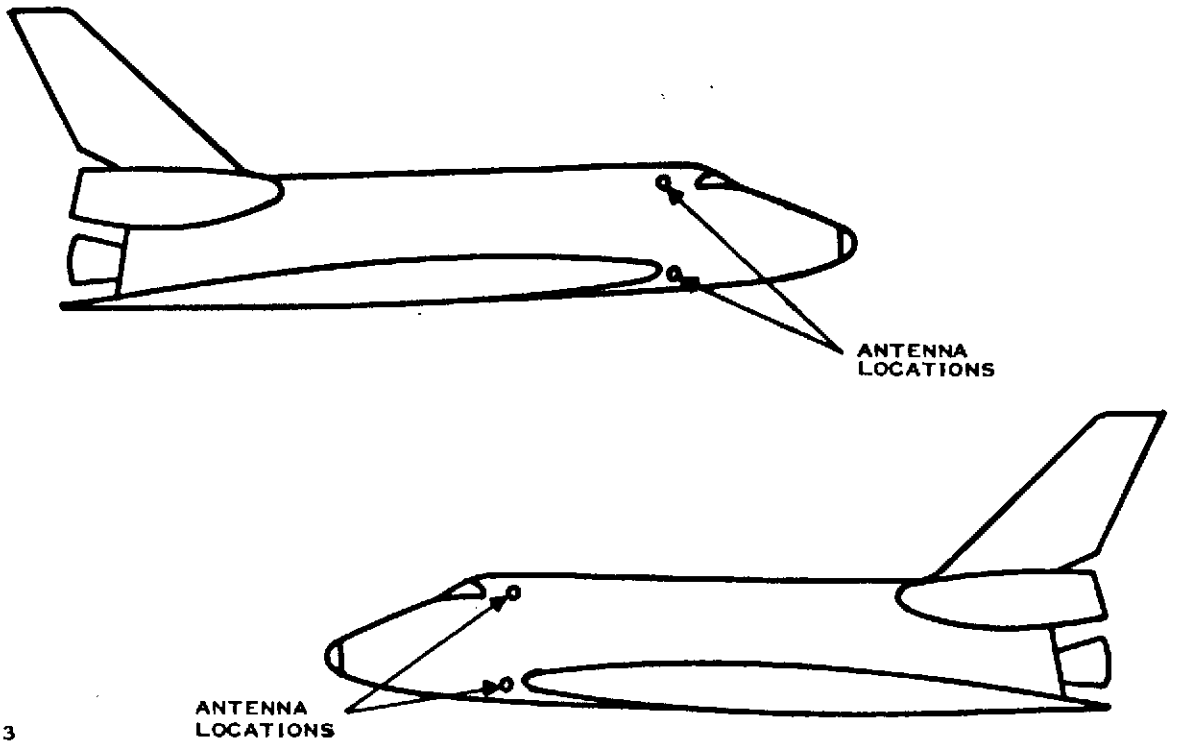
The major comparison between SPACS I and the baseline omni system is shown in Table 11-3. SPACS I shows a clear 10 dB advantage over the baseline on the TDRSS-Orbiter link and a 3.5 dB performance advantage on the Orbiter-TDRSS link. Weight is about equivalent and a substantial power savings results with SPACS I. Since considerable interest exists in a 12 element array, a column is included here for comparison purposes.

Shown in Table 11-4 is the performance of an alternative configuration, a seven and twelve element passive array versus SPACS I. The passive array contains only phasors behind each element. Filtering is employed to retain the single element omni antenna configuration at L-band. Gains shown are stated at the extremities of the 100 X 140 degree cone of coverage.

The SPACS I array shows a 7.8 dB advantage over the passive array for comparable numbers of elements for the TDRSS to orbiter link and retains a 3.5 to 5.5 dB advantage over the passive array on the orbiter to TDRSS link.

C. BREADBOARD SPACS I ARRAY

Photographs of the SPACS I breadboard array are shown in the following photographs. The antenna, RF manifolds, and outer Transmit/Receive module have been tested under this contract and this data has already been reported in previous sections. Shown in Figure 11-3 is the breadboard array front view from the antenna element side. The entire front face is coated with white epoxy radome paint for moisture protection. Shown in Figure 11-4 is a side view of the complete array. The DC and RF connectors are shown. This array is mounted flush against the vehicle thermal protection skin. The mounting ring shown connects to a array support structure in the vehicle.



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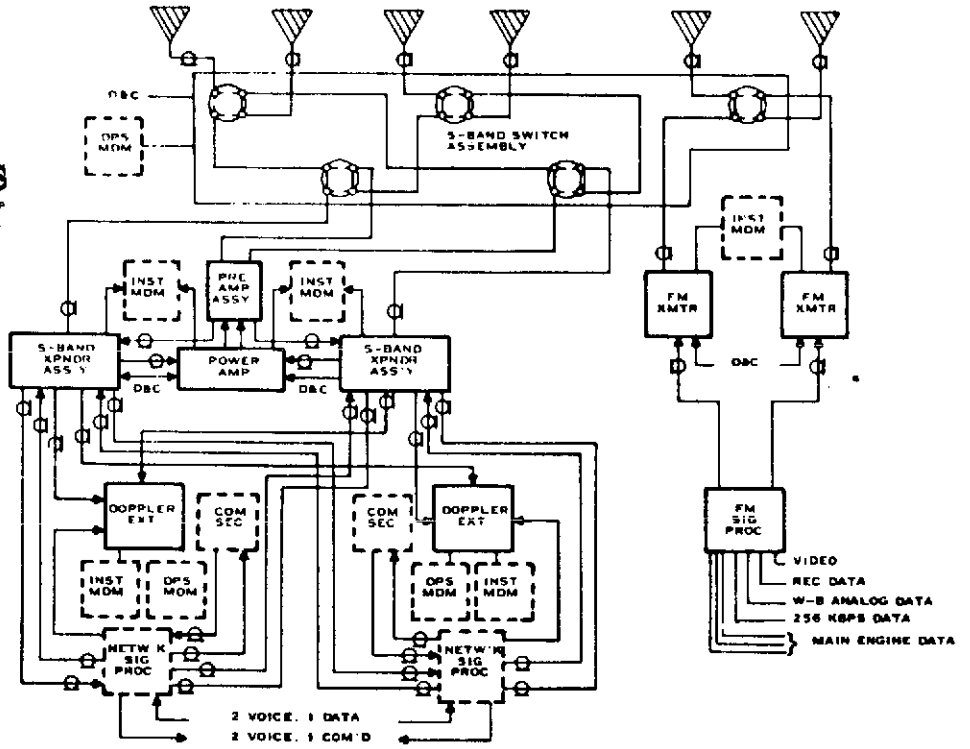

Figure 11-2. S-Band Baseline Antenna System

Table 11-3. Major Parameters - Active Array (SPACS I) Versus Baseline System

	Baseline	SPACS (7 Element)	SPACS (12 Element)
Gain/Noise Temperature	-32 dB°K	-21.7 dB°K	-19.4 dB°K
EIRP	16.9 dBW	19.5 dBW	24.1 dBW
Weight*	75 Pounds	80 Pounds	100 Pounds
DC Power	415 Watts	196 Watts	320 Watts

* This weight does not include weight budgets for the liquid cooling which is required by all three antenna arrays.

Table 11-4. Active Versus Passive Array Performance

Active Array (SPACS I) Receive Performance	7 Elements	12 Elements
Receive Gain	5.5 dB	7.8 dB
Noise Temperature	27.2 dB°K	27.2 dB°K
G/T	-21.7 dB/°K	-19.3 dB/°K
Transmit Performance		
Transmit Gain	6.0 dB	8.3 dB
Transmit Power (3.2 Watts/Module)	13.5 BW	15.8 BW
	19.5 dBW	24.1 dBW

Passive Array (Alternate Scheme) Receive Performance	7 Elements	12 Elements
Receive Gain	5.5 dB	7.8 dB
Phasor/Combiner Loss	-3.0 dB	-3.0 dB
Cable & Switch Loss	-4.9 dB	-4.9 dB
Preamp Temperature	27.1 dB°K	27.1 dB°K
	-29.5 dB/°K	-27.2 dB/°K
Transmit Performance		
Transmit Gain	6.0 dB	8.3 dB
Phasor/Combiner Loss	-3.0 dB	-3.0 dB
Cable/Switch Loss	-7.5 dB	-7.5 dB
Power Amplifier Output	20.5 dBW	20.5 dBW
	16.0 dBW	18.3 dBW

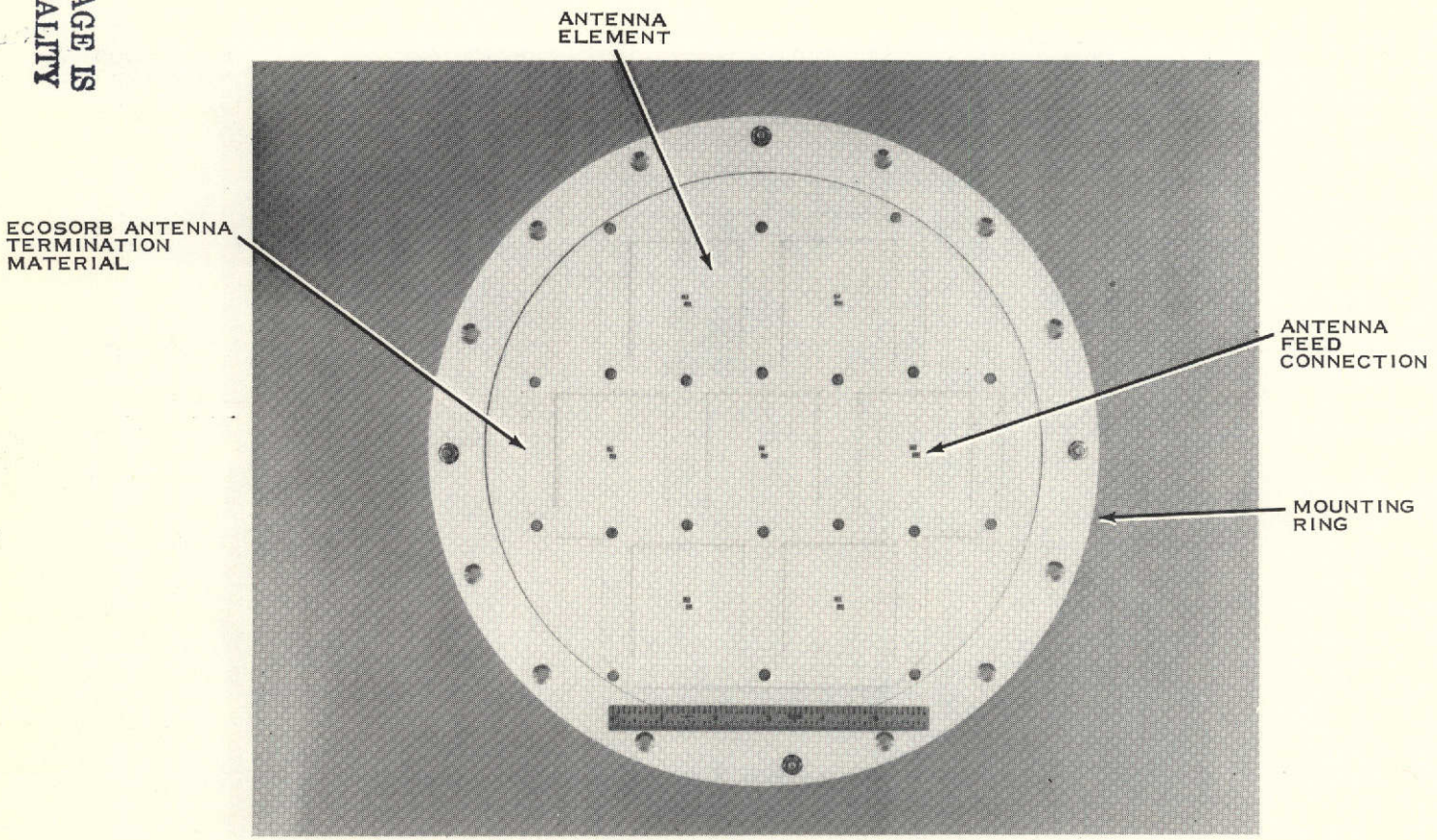

Figure 11-3. Breadboard Array (Front View) Antenna Side

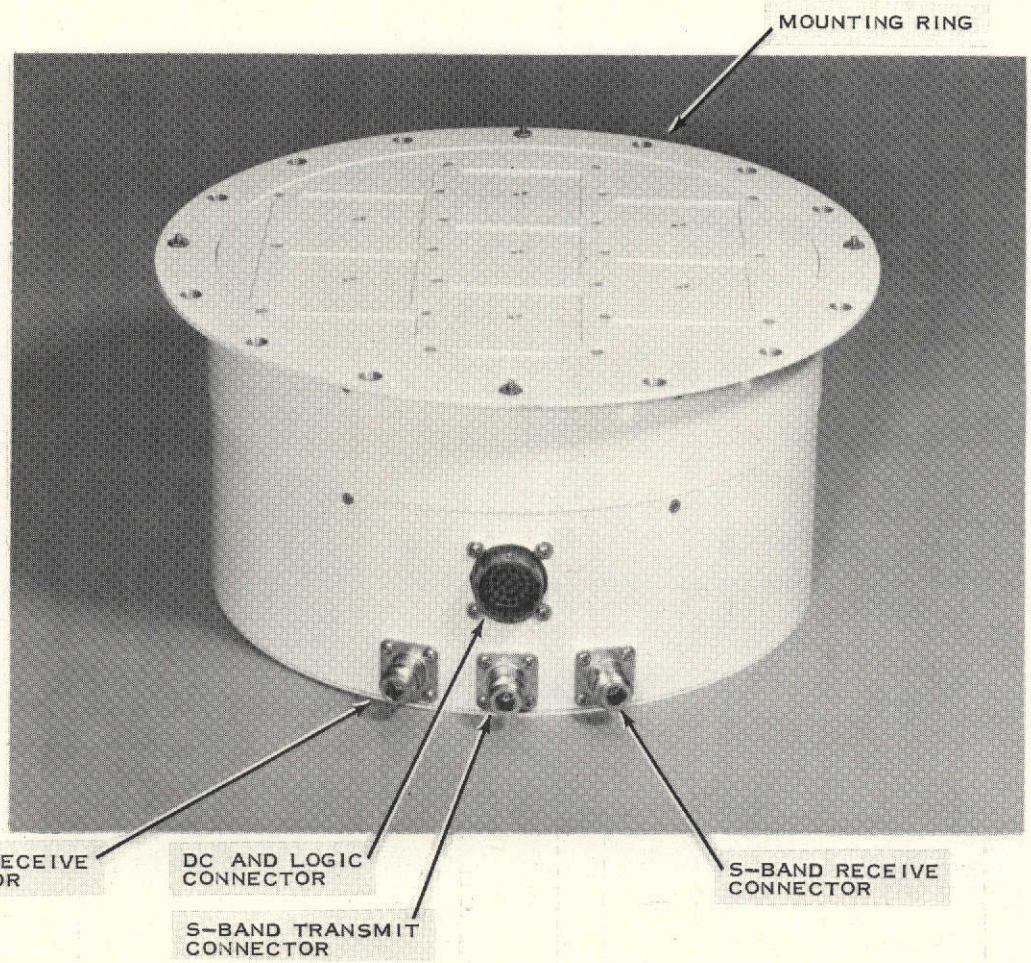

Figure 11-4. Breadboard Array Side View

Shown in Figure 11-5 is a view of the array with dust cover and cables removed. The heat sink plate and manifold connectors are shown. In an actual flight model a heat exchanger will be mounted under the thermal plate below the modules and be an integral part of the thermal plate. Figure 11-6 shows the backside of the array with end plate removed. The cables, connectors, and module are shown in place. Shown in Figure 11-7 is a back view of array with the end plate in place. This end plate is used as a dust cover and a module support in the lateral direction.

D. RISK AREAS AND IMPROVEMENTS

The only possible risk areas for a SPACS I type array is in the areas of thermal environment and vibration specifications. Under the present thermal boundary conditions defined for the array under this contract, a low volume liquid loop is required from the vehicle to cool and heat the array to keep it in its required temperature range. With this liquid loop, all worst case missions can be met. Should it not be possible to supply a liquid loop, several worst case hot temperature conditions could not be met but the majority of normal (nominal) flight missions could be met using an array self-contained liquid loop mounted to the bondline of the aircraft.

Further thermal definition and study should be conducted in coordination with NASA thermal designers to work out all boundary conditions and thermal design methods. The thermal liquid loop is not a great risk, but more design work needs to be done to complete all design details and control methods.

The vibration requirements during reentry and launch could be a problem depending upon the level of vibration and axis of vibration. The present SPACS I array is designed for use in fighter type aircraft (MIL-E-5400 vibration specifications). Further study, definition and design needs to be done to ensure the SPACS flight model would meet all NASA Shuttle vibration requirements. This does not appear to be a real risk area.

Numerous improvements on the SPACS I breadboard unit can be made to further improve its mechanical, electrical and reliability performance. It was not the intent of this research contract to build a flight qualified piece of hardware. Some of the areas for future improvements are reduced system weight, lower system power (higher efficiencies in module), lower system noise temperature, and increased antenna gain. With further work, all of these areas can be improved.

E. SUMMARY

The initial work on this development was formulated in the fall of 1973 during a technical discussion at NASA Johnson Space Center. The contract known as SPACS I, NAS9-14196 was initiated in early summer of 1974 for development of the antenna, feed networks and prototype module. In early 1975 subsequent scope was added which called for the construction of additional modules. That additional scope is shown in the schedule in Table 11-5.

The development of the SPACS array is an outgrowth of the technology developed for NASA MSFC under contract number NAS8-25847 by Texas Instruments

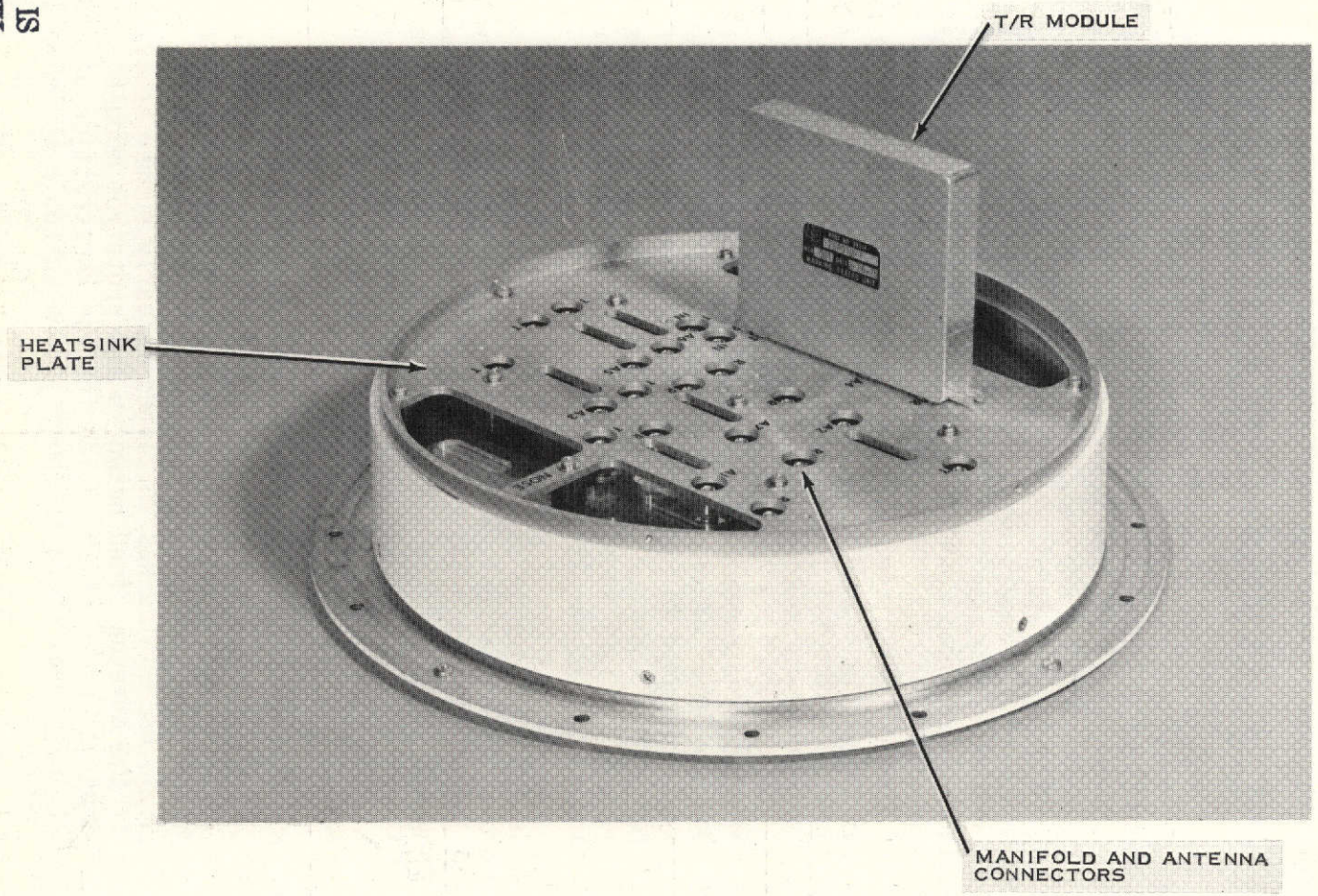

Figure 11-5. Breadboard Array (Dust Cover Removed)

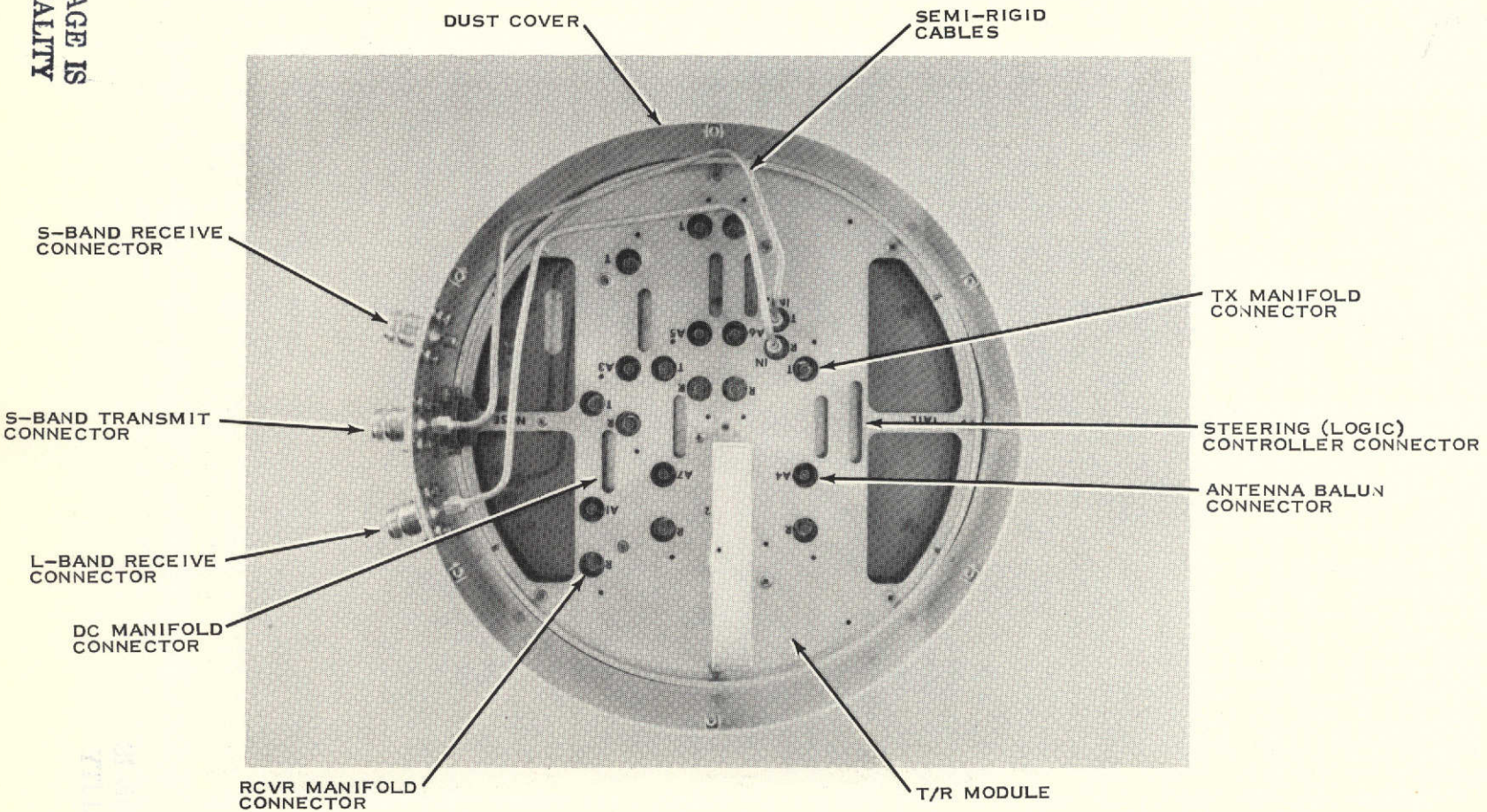

Figure 11-6. Breadboard Array (Back View) - End Plate Removed

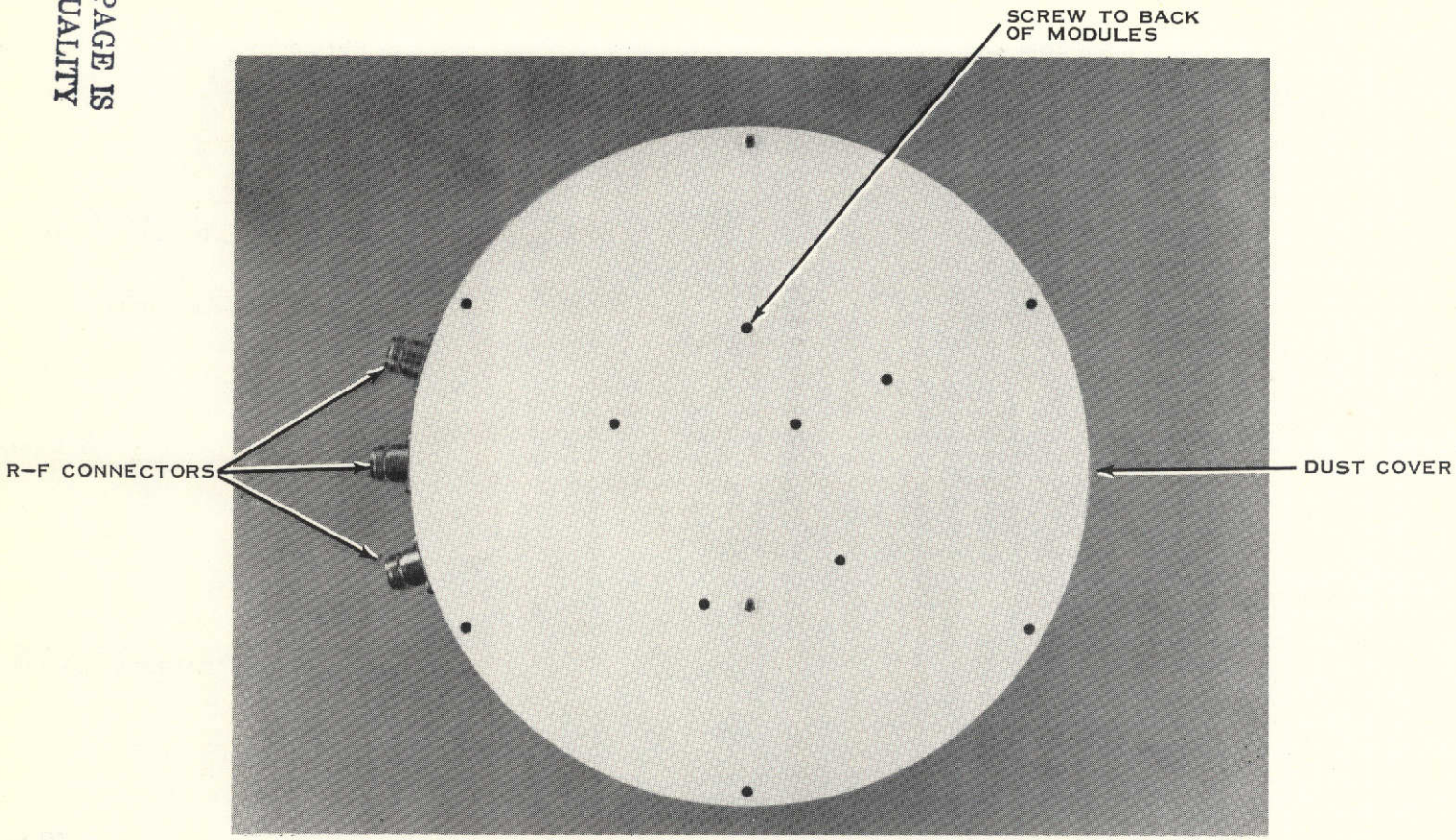

Figure 11-7. Breadboard Array (Back View)

Table 11-5. SPACS Schedule

CURRENT STATUS (12 March 1975)

SPACS I Program

Developed and Tested

- 7 Element Antenna
- RF Feed Networks
- Prototype Module

In Preparation

- Final Report

SPACS II Program

Deliverable Items

- Development and Delivery of 6 additional modules
- Development of a DC Feed Network

Schedule

Contract Received	-	3 January 1975
Receive all parts	-	15 April 1975
Complete Module Assembly and Test	-	15 May 1975
Complete DC Feed Network	-	15 May 1975
Complete Boresight Test	-	15 June 1975
Final Report	-	2 July 1975

and the hardware under this MSFC contract was utilized to the maximum extent possible.

This SPACS I program was very successful and the majority of all design goals were met. The system design outlined and detailed in this final report appears to be a very competitive approach for the S-band communication system for the Space Shuttle. In a great many areas, the SPACS system offers significant advantages over omni and passive phased array systems.

The areas to be developed in the future are (1) a triplexer module, (2) a steering (logic) controller and (3) DC power conditioner and coordinate converter unit. Texas Instruments will welcome the opportunity to expand the technical foundation laid in this effort. We are confident that continued development of the type of spacecraft antenna array described herein will lead to a very useful flight subsystem applicable to a number of spacecraft uses including (1) Space Shuttle, (2) Space Tug and (3) Shuttle Payload Experiments.

APPENDIX A

APPLICATION		REVISIONS			
NEXT ASSY	USED ON	LTR	DESCRIPTION	DATE	APPROVED
	1207	A	Definition In Tables	9/26/75	DRP

SPACS - BREADBOARD SEVEN ELEMENT

ANTENNA ARRAY TEST PROCEDURE

AND DATA SHEETS

REF: NASA/JSC HOUSTON, TEXAS

CONTRACT: NAS9-14196

REV																																		
SHEET																																		
REV STATUS OF SHEETS	REV																																	
	SHEET																																	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
ANGLES ±1°
3 PLACE DECIMAL±.010
2 PLACE DECIMAL±.02

IDENTIFYING NUMBERS SHOWN IN PARENTHESES FOR REFERENCE ONLY

INTERPRET DWG IN ACCORDANCE WITH MIL-STD-100

	DWN	DATE
	CHK D. L. Smith	1/31/75
	ENGR R. Montgomery	1/31/75
	QA	
	APVD	
	CONTR NO	
	DESIGN ACTIVITY RELEASE	

TEXAS INSTRUMENTS
INCORPORATED
Equipment Group Dallas, Texas

SPACS BREADBOARD SEVEN ELEMENT
ANTENNA TEST PROCEDURE AND DATA SHEETS

SIZE	CODE IDENT NO	DRAWING NO
A	96214	SKDD101
SCALE		SHEET 1

TI-9923-C

SPACS I TESTING

I. INTRODUCTION

The purpose of this document is to describe the test procedure for the SPACS seven element square spiral array for its radiation characteristics. A drawing of the array is shown in figure 1. The array is mounted in a large curved ground plane shown in figure 2.

II. PATTERN TESTS

For purposes of obtaining antenna patterns the equipment will be arranged as shown in the block diagram in figure 3. Data will be taken using a rotating linearly polarized transmitting horn in order to display axial ratio.

Table 1 gives the planes of cut and frequencies of the patterns to be measured. The geometry defining ϕ is shown in figure 4. These patterns allow one to obtain sidelobe, beamwidth, and axial ratio information. Additionally, the central element patterns will form the basis for calculating additional scanned array patterns.

III. GAIN TESTS

In order to measure gain the same equipment arrangement shown in figure 3 will be used with one exception. Since a comparison with a standard gain horn is necessary we modify the arrangement as shown in figure 5. The RF switch will be calibrated on an HP network analyzer over the SPACS I frequency bands. Since the standard gain horn (SGH) will be mounted on the rear of the ground plane, one need only switch the RF and rotate the positioner 180° in order to obtain a comparison. Since the gain of the SGH is greater than the SPACS array, linearity in the RF and IF sections should be checked while receiving with the SGH. These linearity checks shall be recorded. Table 2 gives the frequencies at which measurements will be made. Frequencies in addition to the edge frequencies of the bands are required to insure that the measurement is good and that the array has no undue frequency sensitivity due to some mechanical defect. Since there are two separate manifolds - one for transmit and one for receive - one must specify the manifold with which measurements will be made. The manifolds will be characterized by separate measurements on the HP network analyzer. Table 2 also includes all the necessary data reduction for calculating the gain. In this instance, the gain is referred to a matched circularly polarized isotropic source. This gain is related to the axial ratio and linear gain via

$$G_{cp} = G_{linear} + 10 \log (1+r^2) + \text{Manifold Loss} + \text{Cable Loss}$$

where $r = 10^{-a/20}$, $G_{linear} = G_{SGH} - \Delta_{dB}$

where a = axial ratio in dB and $b = 10 \log (1+r^2)$

Manifold Loss = Measured −8.45dB

SIZE	CODE IDENT NO	DRAWING NO
A	96214	SKDD101
SCALE	REV	SHEET 2

TI-7915C

Here G_{linear} is the gain of the maximum envelope of the rotating linear polarization. a is the difference between the maximum and minimum envelopes. The terminology is explained more clearly in figure 6. Note that in addition to gain vs. frequency data obtained from Table 2, we also obtain axial ratio vs. frequency. Note that for the scanned patterns, two rows are allowed for data. One row is for peak of beam data. The other is for data at exactly 70° or 50°, which ever is appropriate.

IV. COMPARISON OF EXPERIMENT WITH SPECIFICATIONS

The electrical specifications which SPACS I must meet are shown in Table 3. The measured data is obtainable from sections II and III. This data will be entered into Table 3 for comparison purposes.

SIZE	CODE IDENT NO	DRAWING NO
A	96214	SKDD101
SCALE	REV	SHEET 3

TI-7915C

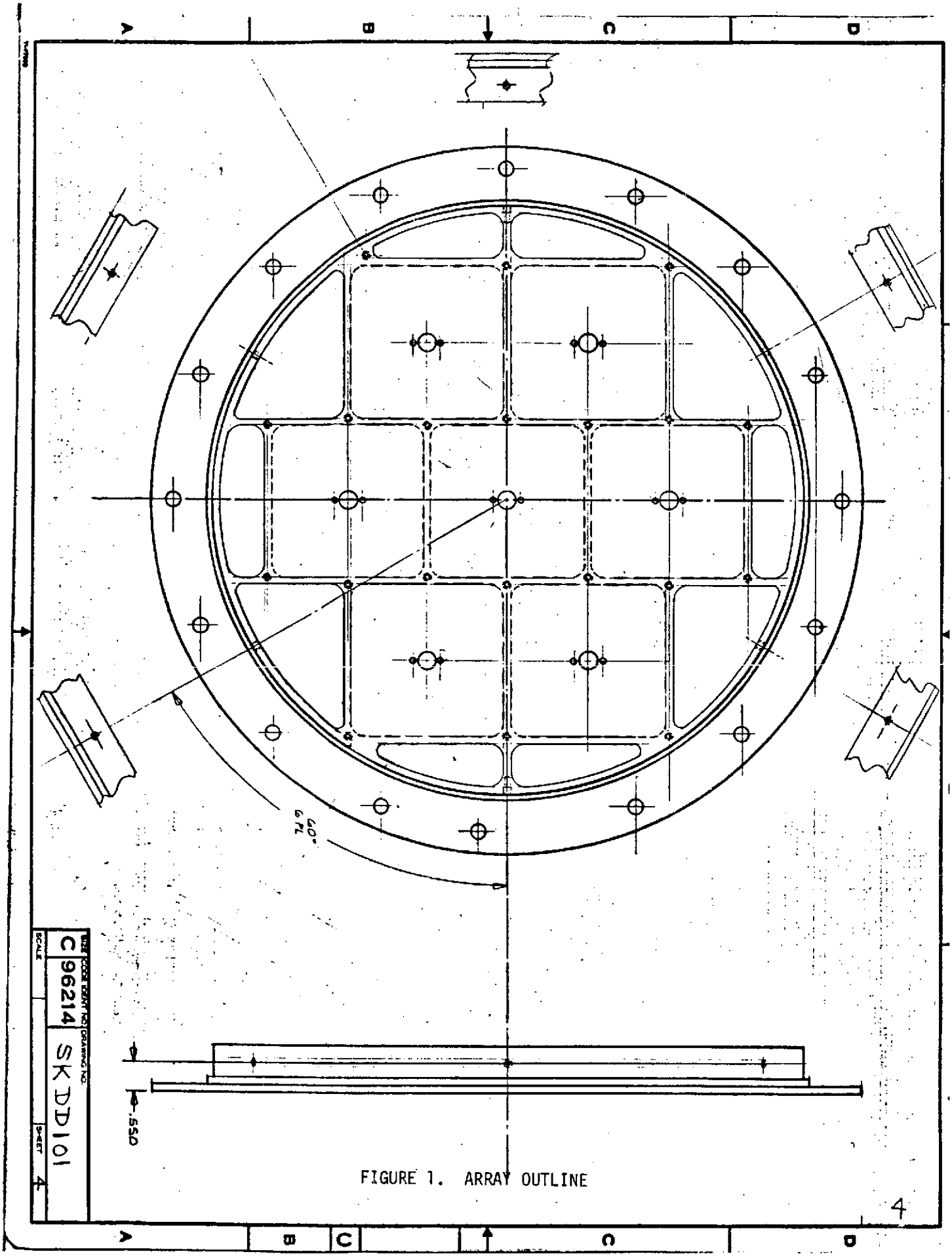

FIGURE 1. ARRAY OUTLINE

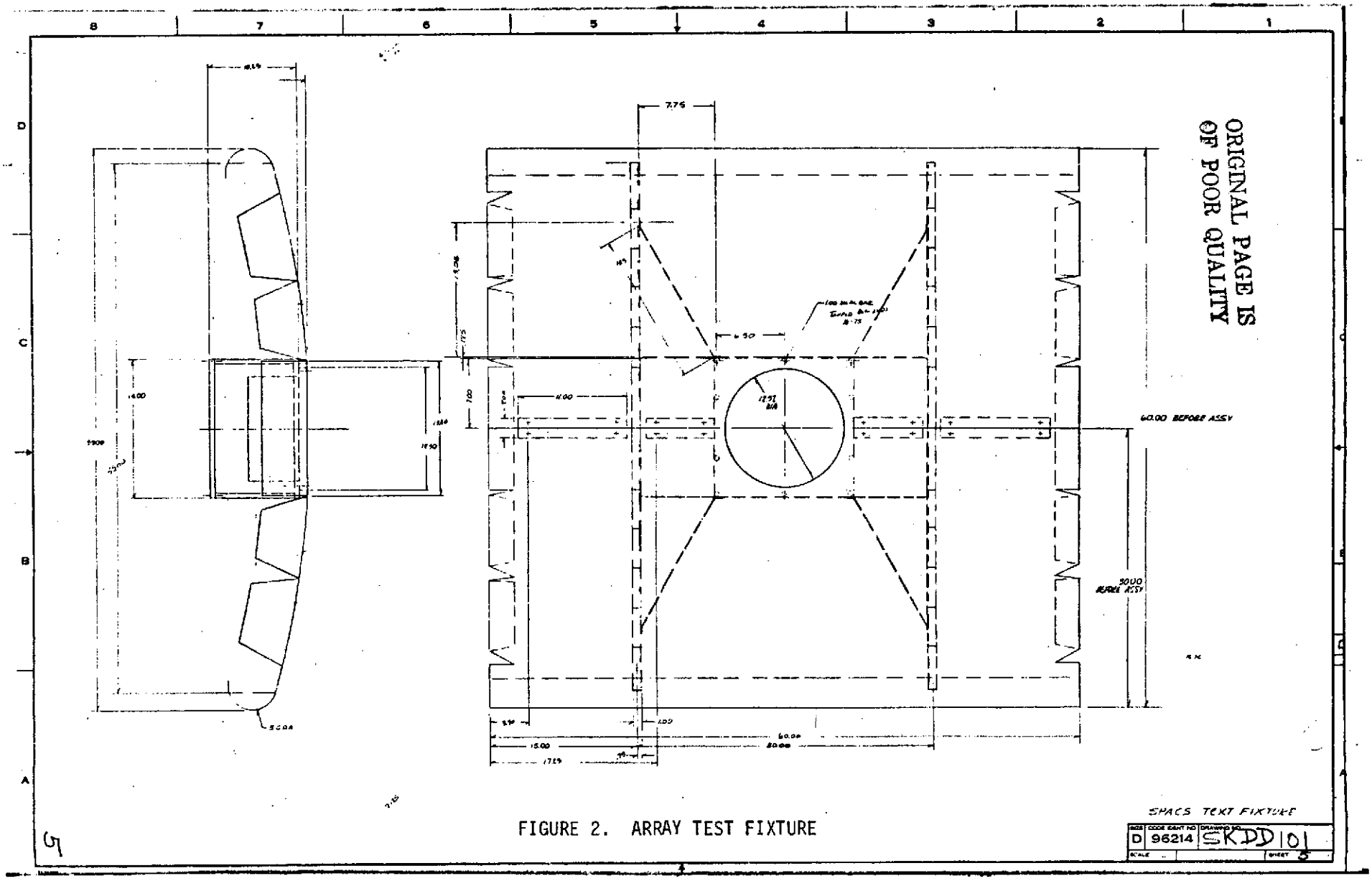

FIGURE 2. ARRAY TEST FIXTURE

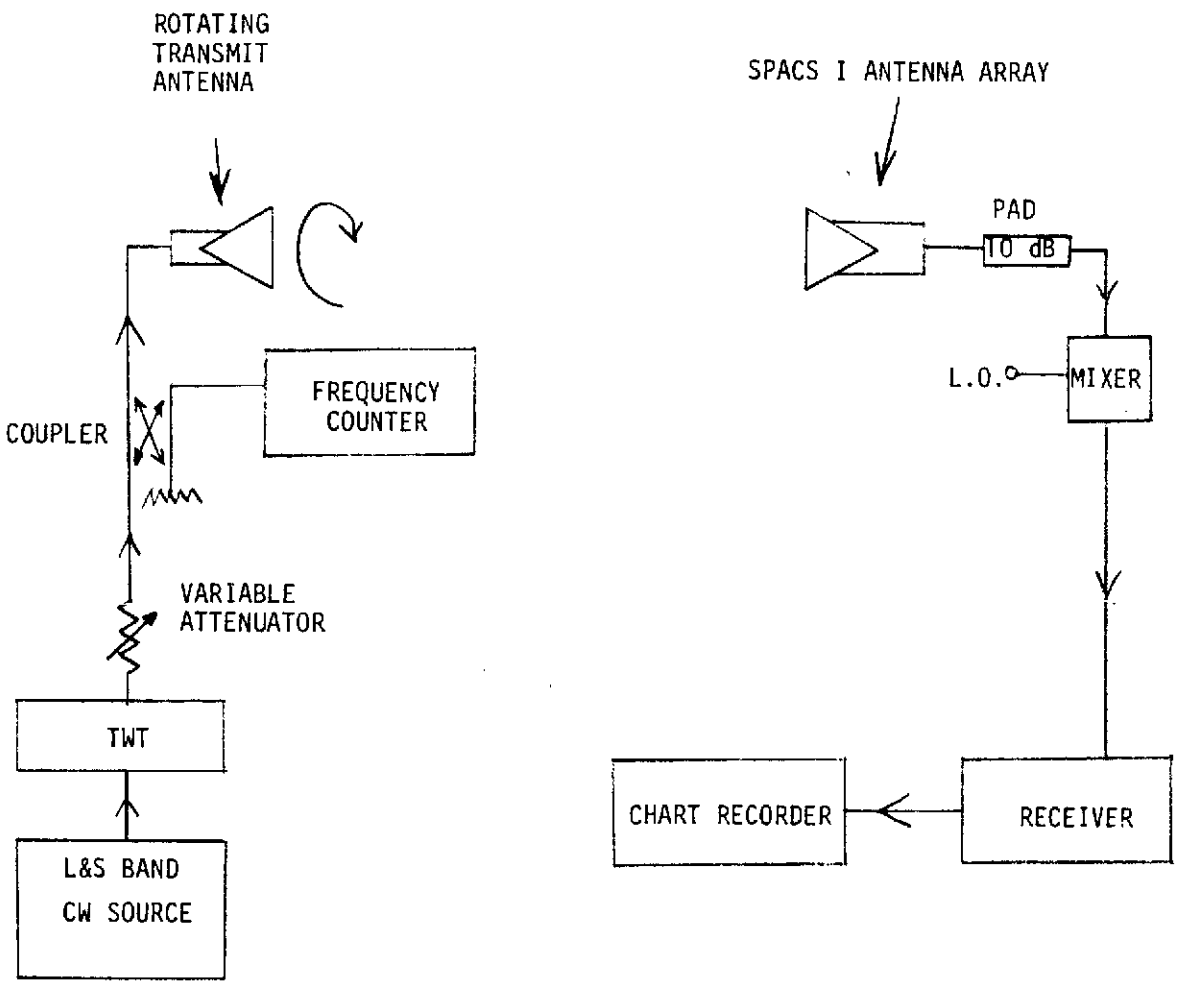

FIGURE 3. EQUIPMENT ARRANGEMENT FOR PATTERN TESTS

SIZE	CODE IDENT NO	DRAWING NO
A	96214	SKDD101
SCALE	REV	SHEET 6

TI-7915C

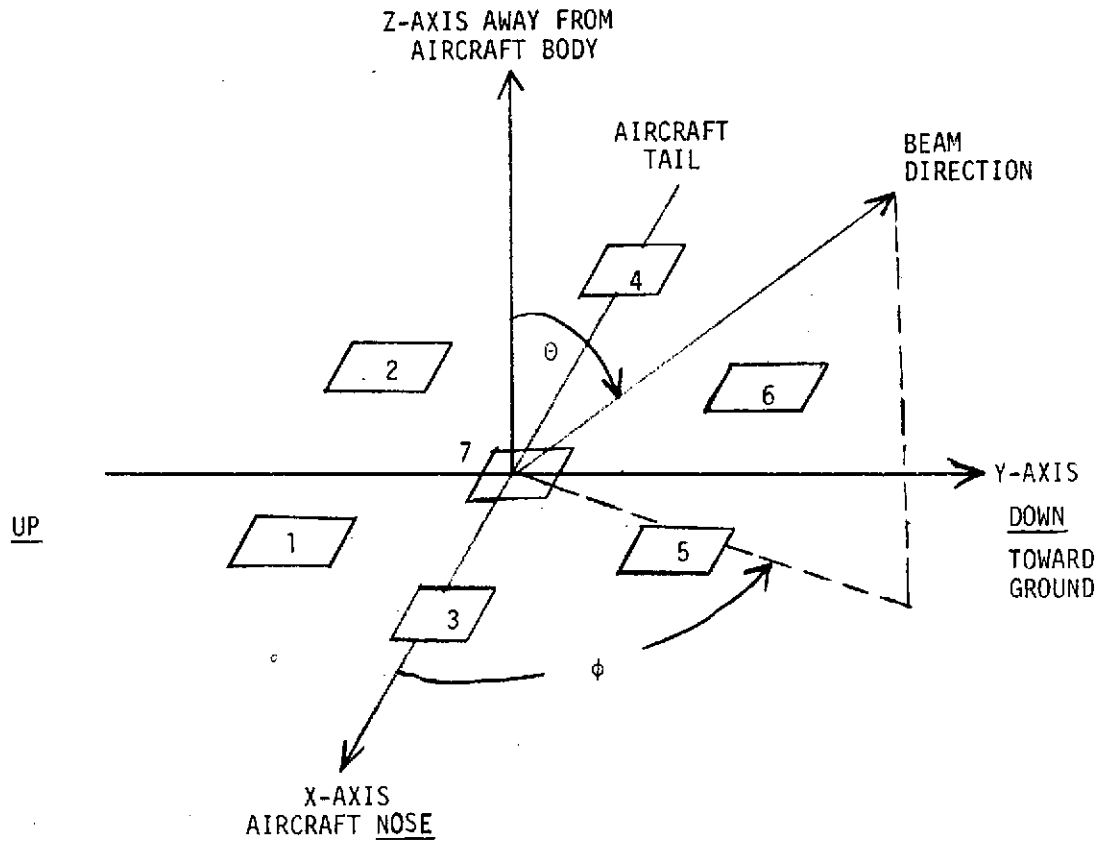

FIGURE 4. ARRAY STEERING GEOMETRY

SIZE	CODE IDENT NO	DRAWING NO
A	96214	SKDD101
SCALE	REV	SHEET 17

TI-7915C

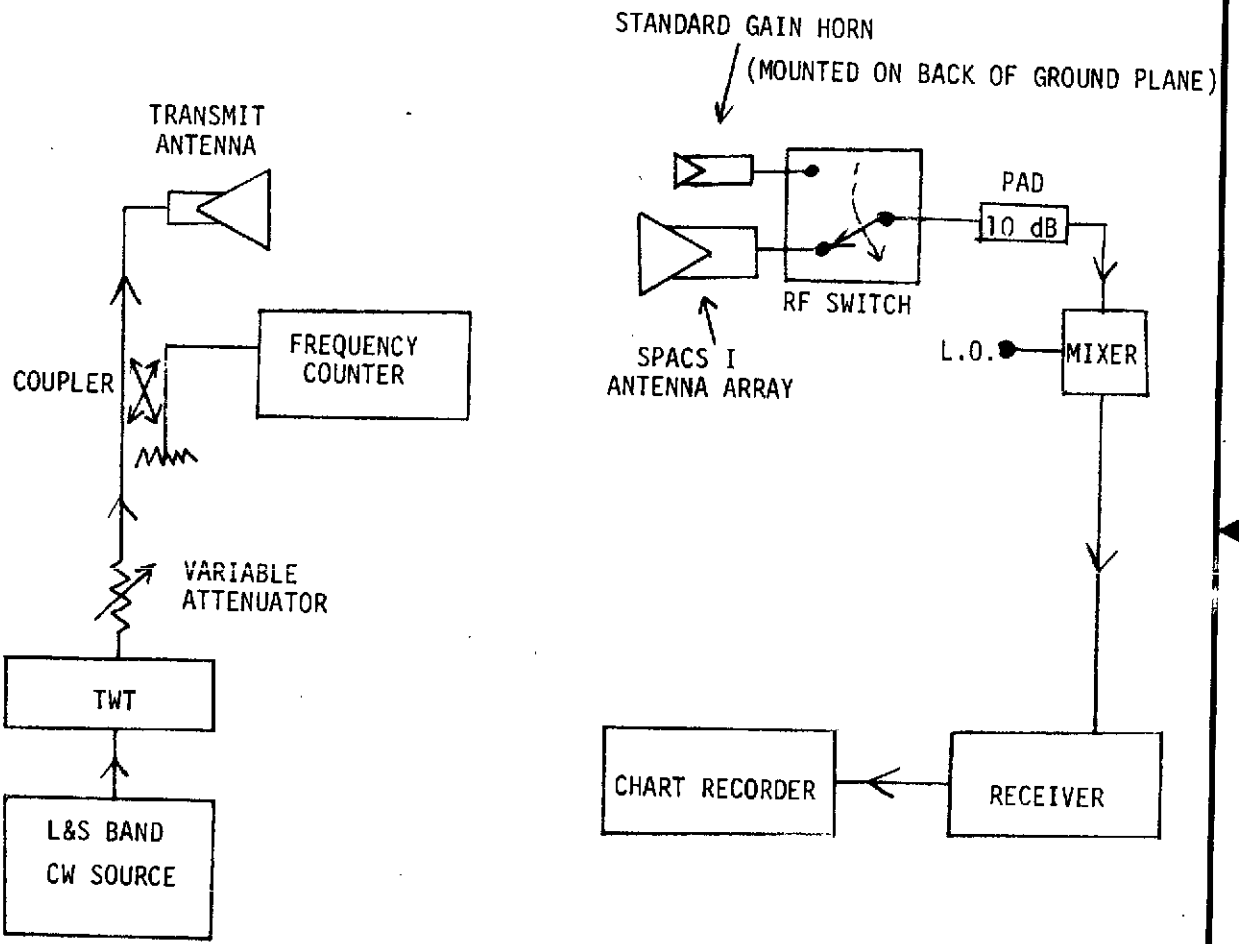

FIGURE 5. GAIN MEASUREMENTS

SIZE	CODE IDENT NO	DRAWING NO
A	96214	SKDD101
SCALE	REV	SHEET 8

TI-7915C

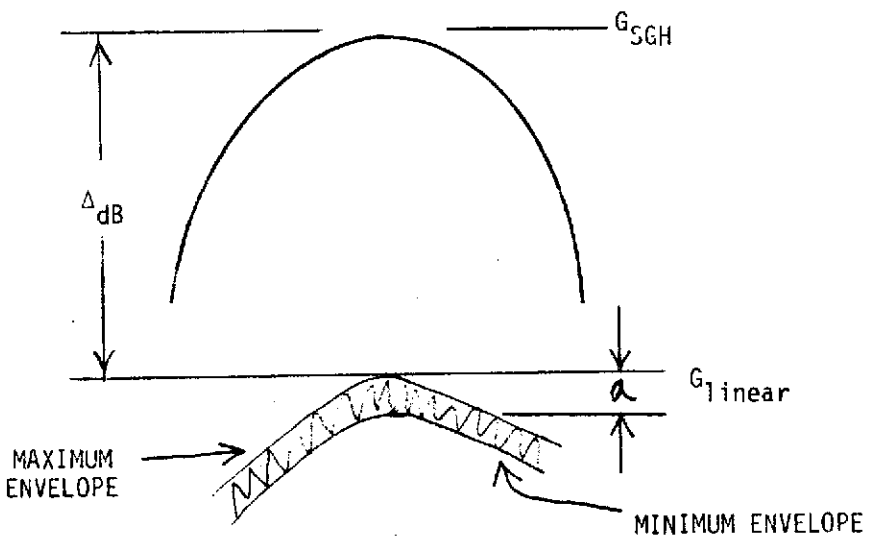

FIGURE 6. GAIN MEASUREMENT TERMINOLOGY

SIZE	CODE IDENT NO	DRAWING NO
A	96214	SKDD101
SCALE	REV	SHEET 9

TI-7915C

	STEERING CABLES	FREQUENCY	PLANE OF CUT	ARRAY OR CENTRAL ELEMENT
1	Boresight	2041.9 MHz	0°	Array
	Boresight	2041.9	90°	Array
	Boresight	2106.4	0°	Array
	Boresight	2106.4	90°	Array
	Boresight	2217.5	0°	Array
	Boresight	2217.5	90°	Array
	Boresight	2287.5	0°	Array
	Boresight	2287.5	90°	Array
2	70° Scan	2041.9 MHz	0°	Array
	70° Scan	2106.4	0°	Array
	70° Scan	2217.5	0°	Array
	70° Scan	2287.5	0°	Array
3	50° Scan	2041.9 MHz	90°	Array
	50° Scan	2106.4	90°	Array
	50° Scan	2217.5	90°	Array
	50° Scan	2287.5	90°	Array
4	N/A	1775.5 MHz	0°	Central Element
		1775.5	90°	Central Element
		1831.8	0°	Central Element
		1831.8	90°	Central Element
		2041.9	0°	Central Element
		2041.9	90°	Central Element
		2106.4	0°	Central Element
		2106.4	90°	Central Element
		2217.5	0°	Central Element
		2217.5	90°	Central Element
		2287.5	0°	Central Element
		2287.5	90°	Central Element

TOTAL PATTERNS = 28

Table 1. Pattern Tests

SIZE	CODE IDENT NO	DRAWING NO
A	96214	SKDD101
SCALE	REV	SHEET 10

TI-7915C

Data Reduced 2/26/75 DKC

TABLE 2. GAIN MEASUREMENTS

$r = 10^{-9/20}$

$b = 10 \log (1+r^2)$

	f(MHz)	STEERING CABLES Loss (dB)	MANIFOLD Loss (dB)	G_{SGH}(dB)		Δ_{dB}	a (dB)	b (dB)	G_{CP}	
		measured	9.75 − 8.45	Scan ∠	Θ					
1	2120.0	BROADSIDE	TRANSMIT	15.98	+0°	9.9	0.6	2.72	12.4	
	2140.0	0.25 dB	1.3 dB	16.07	+0°	9.7	0.4	2.81	12.7	
	2160.0			16.10	+0°	7.2	0.8	2.63	13.1	
	2180.0			16.16	+0°	7.1	0.8	2.63	13.2	
	2200.0			16.21	+0°	7.7	0.6	2.72	12.8	
	2217.5			16.28	+0°	7.8	1.0	2.54	12.0	*
	2240.0			16.30	+0°	8.7	0.3	2.86	12.0	
	2260.0			16.36	−0°	8.6	0.8	2.63	11.9	
	2287.5			16.46	−0°	8.7	0.3	2.86	12.2	*
	2300.0			16.50	−0°	8.8	0.9	2.58	11.8	
	2320.0			16.55	+0°	8.2	0.6	2.72	12.6	
	2340.0			16.60	−0°	8.2	0.9	2.58	12.5	
		measured	9.7 − 8.45	Scan ∠	Θ					
2	2000.0	BROADSIDE	RECEIVE	15.63	+0°	8.9	0.8	2.63	10.9	
	2020.0	0.25 dB	1.25 dB	15.69	+0°	8.6	0.6	2.72	11.3	*
	2041.9			15.76	−0°	8.2	1.0	2.54	11.6	*
	2060.0			15.80	−0°	8.5	1.0	2.54	11.3	*
	2080.0			15.88	−0°	8.1	0.5	2.77	12.1	*
	2106.4			15.93	−0°	7.5	0.6	2.72	12.7	*
	2120.0			15.98	+0°	7.6	0.5	2.77	12.7	*
	2140.0			16.07	−0°	7.4	0.5	2.77	12.9	
	2160.0			16.10	−0°	6.8	0.8	2.63	13.4	
	2180.0			16.16	+0°	6.8	1.2	2.45	13.3	
		measured	9.75 − 8.45	Scan ∠	Θ					
3	2120.0	70°	TRANSMIT	15.98	+70°	12.4	6.0	0.97	6.2	
	2120.0	0.39 dB(P.B.)*	1.3 dB							
	2140.0			16.07	+70°	13.4	6.6	0.86	5.2	
	2140.0	(P.B.)								
	2160.0			16.10	+70°	13.5	5.9	0.99	5.3	
	2160.0	(P.B.)								
	2180.0			16.16	+70°	12.5	7.7	0.68	6.0	
	2180.0	(P.B.)								
	2200.0			16.21	+70	12.4	7.1	0.77	6.3	
	2200.0	(P.B.)								
	2217.5			16.28	+70°	12.1	7.7	0.68	6.6	*
	2217.5	(P.B.)								
	2240.0			16.30	+70°	12.6	7.2	0.76	6.2	
	2240.0	(P.B.)								
	2260.0			16.36	+70°	12.9	6.9	0.81	6.0	
	2260.0	(P.B.)								
	2287.5			16.46	+70°	13.6	6.9	0.81	5.4	*
	2287.5	(P.B.)								
	2300.0			16.50	+70°	12.8	6.8	0.82	6.2	
	2300.0	(P.B.)								

*P.B. means data at peak of beam

SIZE	CODE IDENT NO	DRAWING NO
A	96214	SKDD101
SCALE	REV	SHEET 11

TI-7915C

Data Reduced 2/26/75 DRD

TABLE 2. GAIN MEASUREMENTS CONTD.

	f(MHz)	STEERING CABLES Loss (dB)	MANIFOLD Loss (dB)	G_{SGH}(dB)	θ	Δ_{dB}	a (dB)	b (dB)	G_{CP}	
3	2320.0	0.39 dB	1.3 dB							
	2320.0	(P.B.)		16.55	+70°	12.3	8.7	0.55	6.5	
	2340.0									
	2340.0	(P.B.)		16.60		12.5	9.0	0.51	6.3	
			60° Scan Measurements →		θ					
4	2000.0	70°	RECEIVE	15.63	+60°	13.2	2.9	1.8	5.9	
	2000.0	0.39dB(P.B.)*	1.25 dB							
	2020.0			15.69	+60°	13.0	1.9	2.16	6.5	*
	2020.0	(P.B.)								
	2041.9			15.76	+60°	11.9	3.0	1.96	7.3	*
	2041.9	(P.B.)								
	2060.0			15.80	+60°	12.1	3.9	1.48	6.8	*
	2060.0	(P.B.)								
	2080.0			15.88	+60°	12.1	4.0	1.46	6.9	*
	2080.0	(P.B.)								
	2106.4			15.93	+60°	12.1	3.6	1.57	7.0	*
	2106.4	(P.B.)								
	2120.0			15.98	+60°	12.5	3.7	1.54	6.7	*
	2120.0	(P.B.)								
	2140.0			16.07	+60°	13.4	3.4	1.63	5.9	
	2140.0	(P.B.)								
	2160.0			16.10	+60°	12.5	3.4	1.63	6.9	
	2160.0	(P.B.)								
	2180.0			16.16	+60°	12.2	4.1	1.43	7.0	
	2180.0	(P.B.)								
			50° Scan Measurements →		θ					
5	2120.0	50°	TRANSMIT	15.98	+50°	11.7	1.2	2.45	8.5	
	2120.0	0.45 dB(P.B.)	1.3 dB							
	2140.0			16.07	+50°	12.0	1.2	2.45	8.3	
	2140.0	(P.B.)								
	2160.0			16.10	+50°	11.6	1.4	2.37	8.6	
	2160.0	(P.B.)								
	2180.0			16.16	+50°	11.7	1.6	2.28	8.5	
	2180.0	(P.B.)								
	2200.0			16.21	+50°	11.4	1.4	2.37	8.9	
	2200.0	(P.B.)								
	2217.5			16.28	+50°	12.7	0.6	2.72	8.1	*
	2217.5	(P.B.)								
	2240.0			16.30	+50°	12.1	1.3	2.41	8.4	
	2240.0	(P.B.)								
	2260.0			16.36	+50°	12.3	1.8	2.20	8.0	
	2260.0	(P.B.)								
	2287.5			16.46	+50°	11.8	2.6	1.90	8.3	*
	2287.5	(P.B.)								

*P.B. means peak of beam data.

SIZE	CODE IDENT NO	DRAWING NO
A	96214	SKDD101

SCALE | REV | SHEET 12

TI 7915C

Data Reduced 2/26/75 JRD

TABLE 2. GAIN MEASUREMENTS CONTD.

	f(MHz)	STEERING CABLES loss (dB)	MANIFOLD loss (dB)	G_{SGH}(dB)	θ	Δ_{dB}	a (dB)	b (dB)	G_{CP}	
5	2300.0	0.45 dB	1.3 dB	16.50	+50°	12.5	2.5	1.94	7.7	
	2300.0 (P.B.)									
	2320.0			16.55	+50°	12.5	2.4	1.97	7.8	
	2320.0 (P.B.)									
	2340.0			16.60	+50°	11.6	2.3	2.01	8.5	
	2340.0 (P.B.)									
6	2000.0	50°	RECEIVE	15.63	+50°	11.9	2.0	2.12	7.6	
	2000.0 (P.B.)*	0.45 dB	1.25 dB							
	2020.0			15.69	+50°	12.0	1.9	2.16	7.6	*
	2020.0 (P.B.)									
	2041.9			15.76	+50°	12.5	1.6	2.28	7.2	*
	2041.9 (P.B.)									
	2060.0			15.80	+50°	13.0	0.9	2.55	7.1	*
	2060.0 (P.B.)									
	2080.0			15.88	+50°	12.7	0.8	2.63	7.5	*
	2080.0 (P.B.)									
	2106.4			15.93	+50°	11.9	1.6	2.28	8.0	*
	2106.4 (P.B.)									
	2120.0			15.98	+50°	11.8	1.3	2.41	8.3	*
	2120.0 (P.B.)									
	2140.0			16.07	+50°	11.8	1.1	2.50	8.5	
	2140.0 (P.B.)									
	2160.0			16.10	+50°	11.4	1.4	2.37	8.8	
	2160.0 (P.B)									
	2180.0			16.16	+50°	11.6	1.7	2.24	8.5	
	2180.0 (P.B.)									
7	1760.0	CENTRAL ELEMENT NO MANIFOLD		14.79		16.5	2.6	1.9	0.2	
	1775.5			14.86		16.2	4.8	1.24	-0.1	*
	1800.0			14.93		16.9	1.6	2.28	0.3	
	1820.0			15.00		16.3	1.4	2.39	1.1	
	1831.8			15.05		19.4	3.3	2.01	-0.3	*
	1850.0			15.10		16.2	3.8	1.5	0.4	
	1870.0			15.17						
	2000.0			15.63						
	2020.0			15.69						
	2041.9			15.76						
	2060.0			15.80						
	2080.0			15.88						
	2106.4			15.93						
	2120.0			15.98						
	2140.0			16.07						
	2160.0			16.10						

*P.B. means peak of beam data.

SIZE	CODE IDENT NO	DRAWING NO
A	96214	SKDD101
SCALE	REV	SHEET 13

TI-7915C

Data Reduced
2/26/75
PRD

TABLE 2. GAIN MEASUREMENTS CONTD.

f(MHz)	STEERING CABLES Loss (dB)	MANIFOLD Loss (dB)	G_{SGH}(dB)	Δ dB	a (dB)	b (dB)	G_{CP}
2180.0			16.16				
2200.0			16.21				
2217.5			16.28				
2240.0			16.30				
2260.0			16.36				
2287.5			16.46				
2300.0			16.50				
2320.0			16.55				
2340.0			16.60				

7

*P.B. means peak of beam data.

SIZE	CODE IDENT NO	DRAWING NO
A	96214	SKDD101
SCALE	REV	SHEET 14

FC 79150

Table 3. Specification Comparison With Experiment

Specification	Experiment	Comment
Minimum broadside receive gain, 11.5 dB		
Minimum 60° scan receive gain, 5.5 dB		Extrapolated from 0° and 70°
Minimum broadside transmit gain, 12 dB		
Minimum 70° scan transmit gain, [redacted] 4.5 dB		
Beamwidth (nominal) 40°		Experiment will record minimum and maximum beamwidths in receive and transmit for ϕ=0° and 90° from broadside steering.
Minimum L-band gain, (boresight), [redacted] 0 dB		Central Element

SIZE	CODE IDENT NO	DRAWING NO
A	96214	SKDD101
SCALE	REV	SHEET 15

TI-7915C

APPENDIX B

A

APPLICATION		REVISIONS			
NEXT ASSY	USED ON	LTR	DESCRIPTION	DATE	APPROVED
	1207	A	Changed Paragraphs III & IV and power levels of Table I	2/24/75	DRP

SPACS - BREADBOARD TRANSMIT/RECEIVE

MICROELECTRONICS MODULE TEST

PROCEDURE AND DATA SHEETS

REF: NASA/JSC HOUSTON, TEXAS

CONTRACT: NAS9-14196

REV																																
SHEET																																
REV STATUS OF SHEETS	REV																															
	SHEET																															

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
ANGLES ±1°
3 PLACE DECIMAL ±.010
2 PLACE DECIMAL ±.02

IDENTIFYING NUMBERS SHOWN IN PARENTHESES FOR REFERENCE ONLY

INTERPRET DWG IN ACCORDANCE WITH MIL-STD-100

DWN	E. Delzer 2-20-75 (DATE)
CHK	
ENGR	E. Delzer 2/20/75
QA	
APVD	
CONTR NO	
DESIGN ACTIVITY RELEASE	

TEXAS INSTRUMENTS
INCORPORATED
Equipment Group Dallas, Texas

SPACS BREADBOARD TRANSMIT/RECEIVE
MICROELECTRONICS MODULE TEST PROCEDURE
AND DATA SHEETS

SIZE	CODE IDENT NO	DRAWING NO
A	96214	SKDD102
SCALE		SHEET 1 OF 17

TI-8923-C
P1

SPACS I - TRANSMIT/RECEIVE MODULE TESTING

I. INTRODUCTION

The purpose of this document is to describe the test procedure for the SPACS transmit/receive microelectronics module. This measured data is to be compared to the design parameters as defined by paragraph 3.2.3.2 of the contract NAS9-14196.

II. MODULE TRANSMITTER TESTS

The transmitter side of the module will be tested using a Hewlett-Packard Automatic Network Analyzer (ANA) Model 8542A modified for high power measurements. The measurement will be controlled by a Texas Instruments developed software program (APAM1-1, Automatic Power Amplifier Measurement) based upon the HP8540 software series.

The test setup for this transmitter test is shown in Figure 1. An example ANA printout is shown by Figure 2. The device under test shown in Figure 1 will be the transmitter side of the SPACS I breadboard module.

In addition to the data shown by the printout of Figure 2, current on each of the power supply lines (+5V, +12V, and +22 volts) will be recorded from VOM readings at the minimum (0°) phase setting for each power level. All of this data will be recorded on the data sheet in the Appendix labeled Table I. The data will be taken at room temperature (25°C) only.

III. MODULE RECEIVER TESTS

The receiver side of the module will be tested using a Hewlett-Packard Automatic Network Analyzer (ANA) model 8542A under small signal conditions. The measurement will be controlled by a HP software program AGS03.

This measurement will use the same test setup as shown in Figure 1 with the exception of substitution of the HP 8746 Test Unit for the HP 8745 Test Unit. An example printout of the type of data measured is shown by Figure 3. The device-under-test shown in Figure 1 will be the receiver side of the SPACS I breadboard module.

In addition to the data shown by the printout of Figure 3, current on the power supply lines (+12V and +5 volts) will be recorded from VOM readings at the minimum (0°) phase setting. Power input to the antenna connector of the module will be -40 dBm to insure that the receiver amplifier is being operated in its linear (uncompressed) region.

All of this data will be recorded on the data sheet in the Appendix labeled Table II. The data will be taken at room temperature (25°C) only.

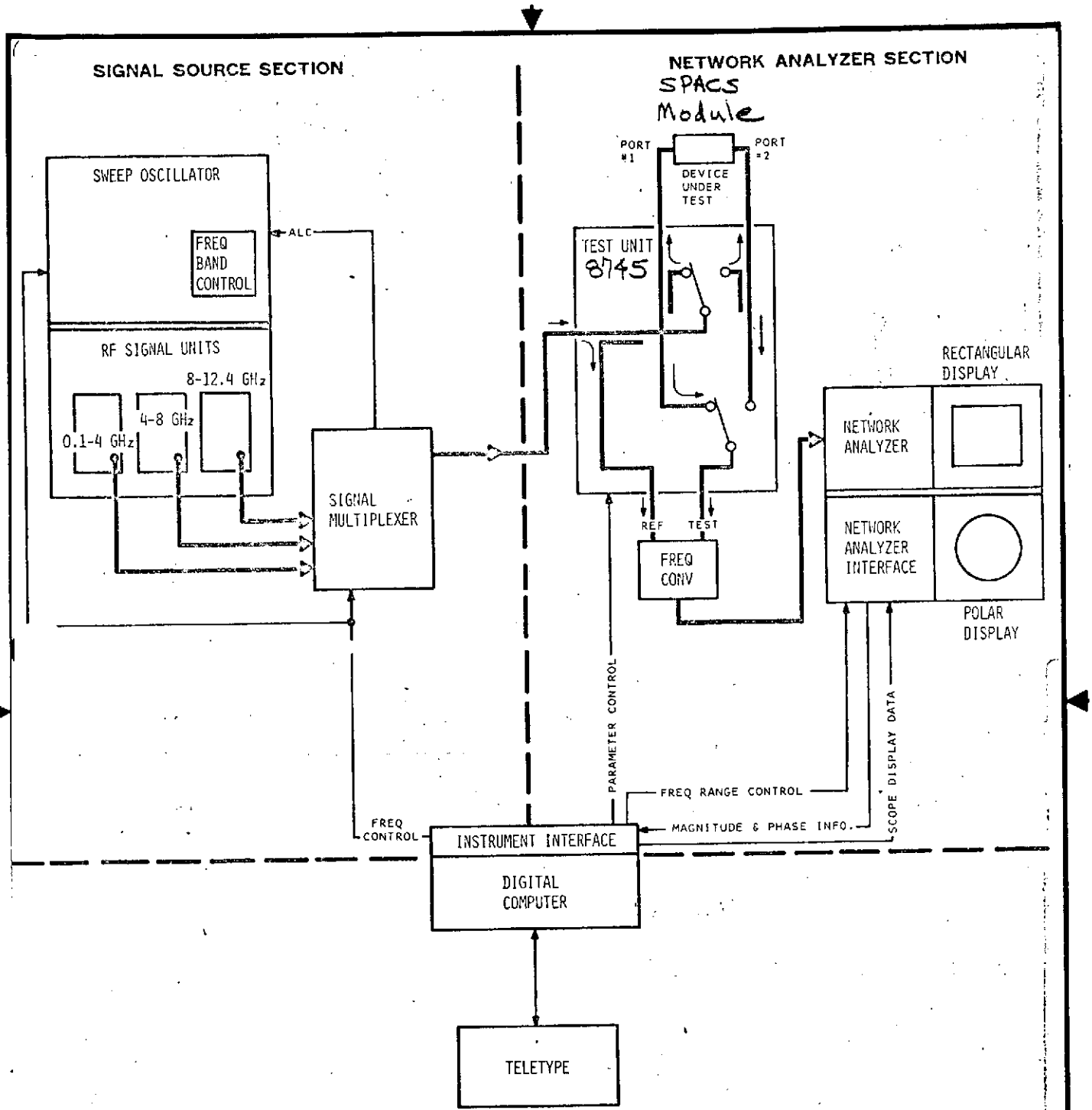

FIGURE 1. AUTOMATIC NETWORK ANALYZER SYSTEM (HP 8542 A)

SIZE	CODE IDENT NO	DRAWING NO
A	96214	SKDD102
SCALE	REV	SHEET 3

TI-7915C

GPHDE = 1624.336

TASK, TYPE? 2,1

NEW MEAS? Y

CONN DEVICE...TRW/ESA 20V,5V...11 DEGREES C

FREQ	REFL	VSWR	P IN	GAIN	PHASE	P OUT
		POWER LEVEL = 6.00 DBM				
2100.000	.170	1.409	5.97	-28.82	79.7	-22.85
2110.000	.157	1.373	5.97	-27.14	73.6	-21.17
2120.000	.140	1.324	5.97	-25.42	80.1	-19.45
2130.000	.118	1.268	6.01	-18.42	119.1	-12.41
2140.000	.060	1.128	5.97	19.41	84.4	25.37
2150.000	.081	1.177	5.97	19.47	73.5	25.43
2160.000	.098	1.217	6.01	19.34	63.1	25.35
2170.000	.112	1.253	6.00	19.16	53.5	25.16
2180.000	.122	1.278	5.97	18.89	43.0	24.86
2190.000	.131	1.300	5.99	18.58	32.6	24.57
2200.000	.138	1.319	6.00	18.18	21.8	24.17
2210.000	.147	1.344	6.00	17.50	11.6	23.50
2220.000	.157	1.372	5.99	16.74	.0	22.72
2230.000	.166	1.399	5.99	16.07	-13.3	22.05
2240.000	.177	1.430	5.99	15.32	-26.9	21.31
2250.000	.188	1.464	6.00	14.36	-41.0	20.36
2260.000	.205	1.516	5.99	12.30	-55.1	18.28
2270.000	.223	1.574	6.00	8.33	-68.9	14.33
2280.000	.236	1.617	5.97	2.04	-85.1	8.00
2290.000	.236	1.619	5.97	-5.00	-103.4	.96
2299.999	.231	1.600	5.97	-10.57	-129.6	-4.60
		POWER LEVEL = 7.00 DBM				
2100.000	.172	1.416	6.99	-28.79	86.0	-21.80
2110.000	.053	1.111	6.99	18.23	119.1	25.22
2120.000	.047	1.100	7.00	18.31	104.6	25.31
2130.000	.059	1.125	7.00	18.40	92.0	25.40
2140.000	.076	1.164	7.01	18.41	80.6	25.42
2150.000	.091	1.201	7.00	18.47	70.0	25.47
2160.000	.104	1.231	7.01	18.42	60.0	25.43
2170.000	.113	1.255	6.96	18.36	50.2	25.33
2180.000	.120	1.273	6.98	18.22	40.0	25.20
2190.000	.125	1.285	6.97	18.00	29.5	24.97

Figure 2 – ANA Printout for Transmitter Measurement (APAM 1-1)

SIZE	CODE IDENT NO	DRAWING NO
A	96214	SKDD 102
SCALE	REV	SHEET 4

TI-7915C

TASK? TYPE? S,1

NEW MEAS? Y

CONN DEVICE TRANS MAN HOLES & SPACERS DELRIN INPUT TO PORT 2 3/15/75 DRD

FORWARD:

FREQ	REFL	ANGLE	RTN LS	VSWR	GAIN	PHASE	DELAY
2200.000	.167	-92.0	15.6	1.400	-9.97	131.2	2.578
2210.000	.149	-104.2	16.5	1.351	-9.95	121.9	2.758
2220.000	.132	-115.7	17.6	1.304	-9.95	112.0	2.926
2230.000	.116	-126.7	18.7	1.263	-9.92	101.8	3.774
2240.000	.100	-137.3	20.0	1.223	-9.86	91.8	3.592
2250.000	.084	-147.4	21.5	1.183	-9.78	82.1	2.623
2260.000	.066	-156.7	23.6	1.142	-9.71	72.7	2.594
2270.000	.048	-167.4	26.3	1.101	-9.63	63.3	2.488
2280.000	.032	178.9	29.9	1.066	-9.60	54.4	2.436
2290.000	.018	163.1	34.8	1.037	-9.58	45.6	2.377
2300.000	.008	128.4	41.3	1.016	-9.56	37.0	2.479
2310.000	.009	36.2	40.6	1.019	-9.59	28.1	2.801
2320.000	.019	10.6	34.7	1.038	-9.63	18.7	2.857
2330.000	.025	-.4	32.2	1.050	-9.67	9.2	2.704
2340.000	.029	-12.5	30.8	1.060	-9.70	-.5	2.712
2350.000	.031	-17.3	30.1	1.064	-9.66	-10.3	2.623
2360.000	.031	-21.8	30.2	1.064	-9.59	-19.8	2.497
2370.000	.030	-24.0	30.6	1.061	-9.55	-29.7	2.580
2380.000	.027	-28.4	31.5	1.055	-9.57	-37.8	2.522
2390.000	.025	-15.5	32.0	1.051	-9.62	-46.9	2.583
2399.999	.026	-6.5	31.8	1.053	-9.74	-56.2	2.583

Figure 3 – ANA Printout for Receiver Measurement (AG503)

SIZE	CODE IDENT NO.	DRAWING NO.
A	96214	SKDD 102
SCALE	REV	SHEET 5

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IV. RECEIVER NOISE FIGURE MEASUREMENT

The receiver side of the module will be tested using an AIL Model 75 Automatic Noise Figure Meter and an AIL Model 7010 Noise Generator. This will be a manual test using a calibrated test setup as shown in Figure 4.

This noise figure data will be recorded on the data sheet in the Appendix labeled Table III. The data will be taken at room temperature (25°C) only. This data will be compared to module design goal of 4.87 dB noise figure; the maximum module noise figure requirement is 5.33 dB.

V. RECEIVER COMPRESSION POINT MEASUREMENT

The compression characteristic of the receiver will be tested using a manual calibrated setup as shown in Figure 5.

The 1 dB compression point will be measured and recorded for each of the frequencies shown in Table III of the Appendix. This compression data will be compared to the module requirement of +10 dBm at 1 dB compression point.

VI. MODULE DUPLEX OPERATION TEST

The duplex operation of the module will be checked by operating the transmitter-antenna connector output into a 1.5:1 VSWR load and looking at the output level of transmitter signal coming from the receiver connector. This measurement will be made with a spectrum analyzer as shown in Figure 6.

The 1.5 VSWR load will similate the antenna reflection. This measured transmitter leakage level should be below the receiver 1 dB compression point at the transmitter frequency. (Thus, below +10 dBm output level). This data will also be recorded in Table III.

SIZE	CODE IDENT NO.	DRAWING NO.
A	96214	SKDD102
SCALE	REV	SHEET 6

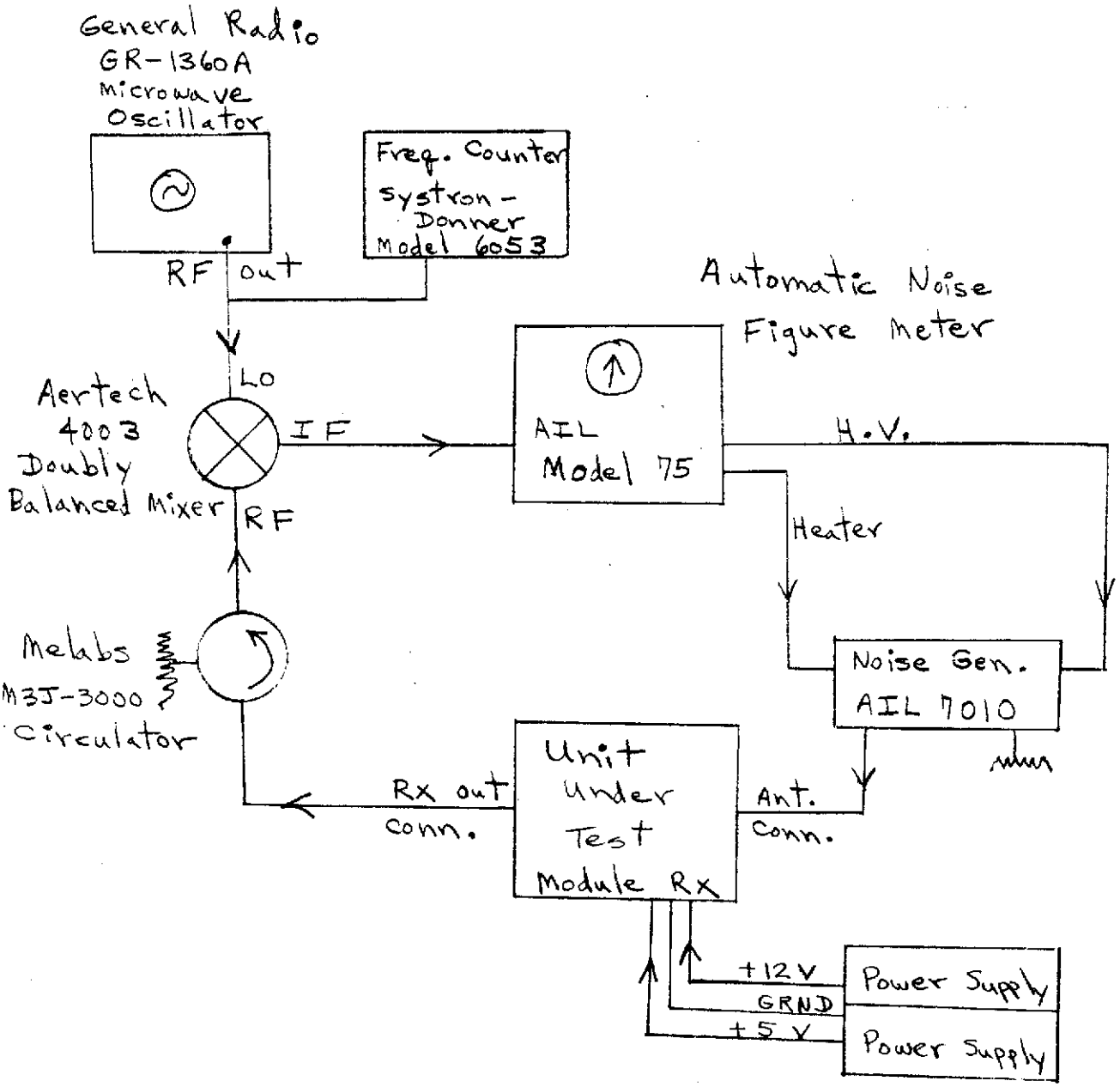

Figure 4 – Receiver Noise Figure Test Setup (Equivalent Equipment may be substituted)

SIZE	CODE IDENT NO	DRAWING NO
A	96214	SKDD102
SCALE	REV	SHEET 7

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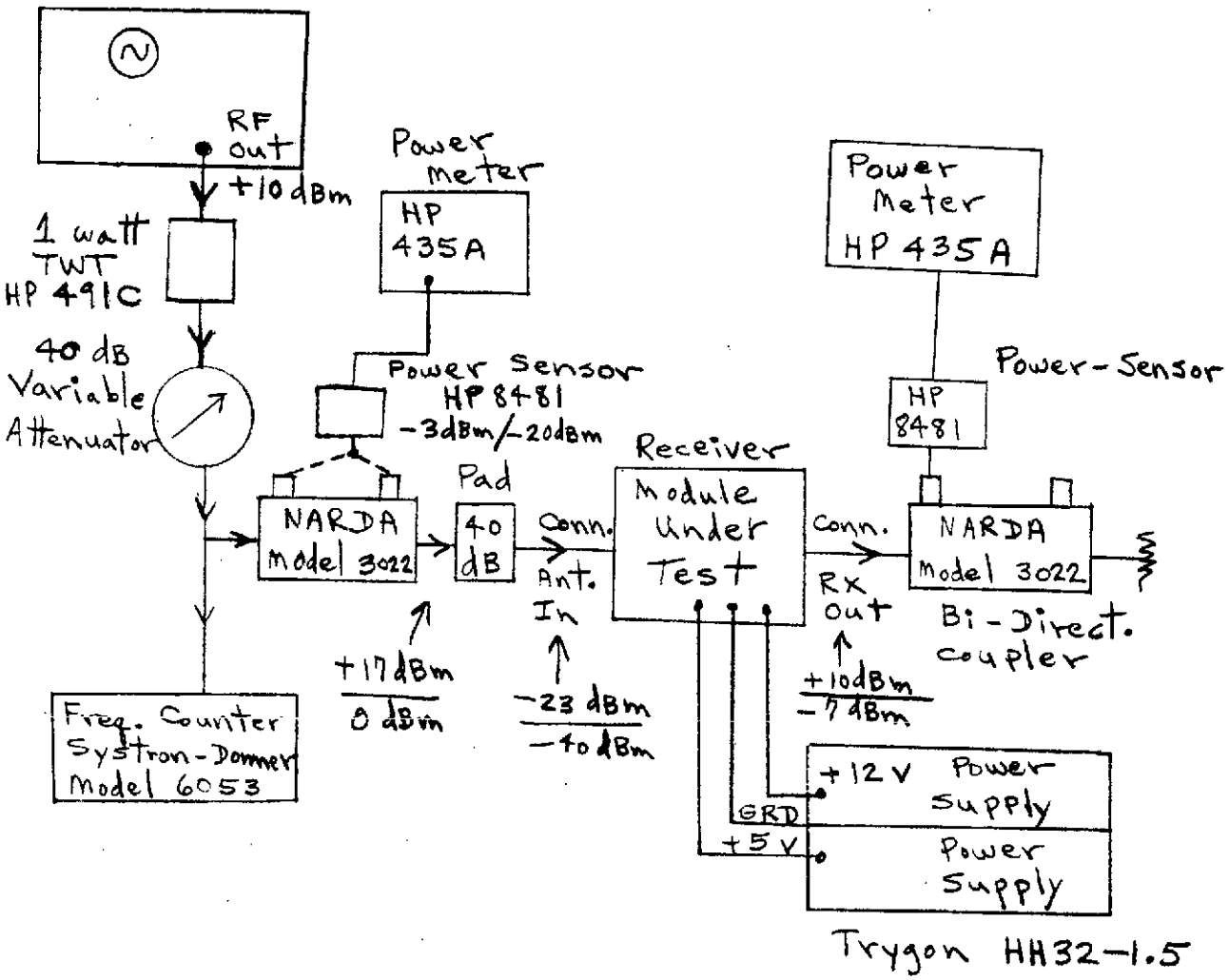

Figure 5 - Receiver Compression (1 dB) Point Test Setup (Equivalent Equipment may be substituted)

SIZE	CODE IDENT NO	DRAWING NO
A	96214	SKDD102
SCALE	REV	SHEET 8

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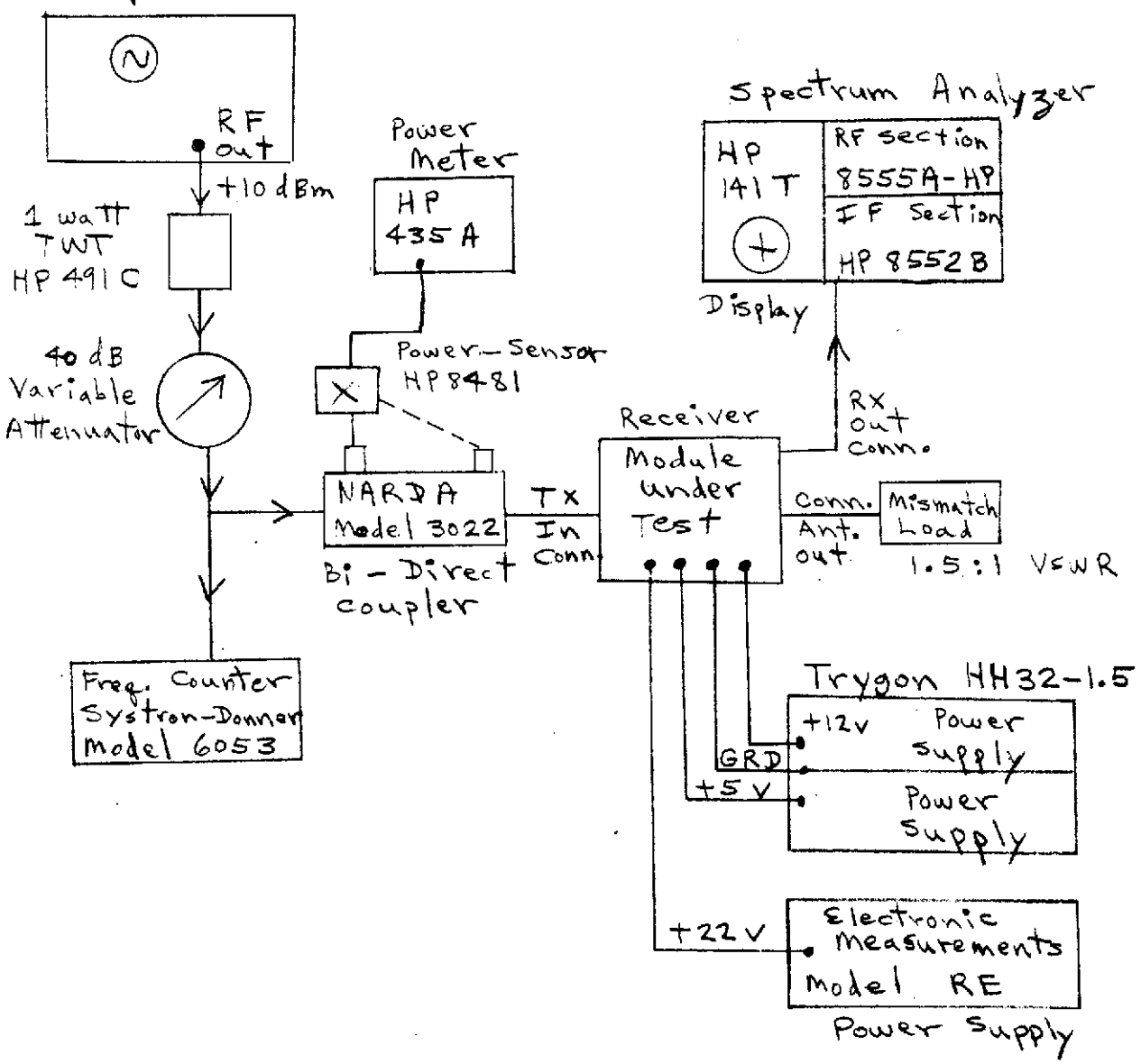

Figure 6 — Module Duplex Operation Test
(Equivalent Equipment May be Substituted)

SIZE	CODE IDENT NO	DRAWING NO
A	96214	SK DD 102
SCALE	REV	SHEET 9

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APPENDIX

SIZE	CODE IDENT NO.	DRAWING NO.
A	96214	SKDD102
SCALE	REV	SHEET 10

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Table I. Recorded Transmitter Data
(Room Temperature Only)

Input Power Level = +12 dBm

Frequency MHz	Commanded Phase Setting Degrees	Measured Phase Setting Degrees	Input VSWR	Power Output dBm	Gain dB	Power Supply* Currents mA
2217.5	0	7.6 (0)	1.125	36.29	24.29	I_{5V} = 73
	45	-27.7 (35.3)	1.191	35.91	23.91	
	90	-78.7 (86.3)	1.527	35.81	23.81	I_{12V} = 41
	135	-110.5 (118.1)	1.378	35.80	23.80	
	180	179.5 (188.1)	1.104	35.55	23.55	
	225	148.5 (219.1)	1.066	35.53	23.53	I_{22V} = 880
	270	99.1 (262.5)	1.206	35.76	23.76	
	315	69.8 (302.8)	1.056	35.71	23.71	
2252.5	0	-179.7 (0)	1.732	36.62	2462	I_{5V} = 73
	45	142.6 (322)	2.088	36.16	24.16	
	90	100.3 (80.)	1.496	36.47	24.47	I_{12V} = 43
	135	52.7 (127.6)	1.184	36.35	24.35	
	180	-2.3 (182.6)	1.424	36.33	24.33	
	225	-38.4 (218.7)	1.241	36.27	24,27	I_{22V} = 880
	270	-85.3 (265.6)	1.132	3639	2439	
	315	-131.9 (312.2)	1.517	36.17	24.17	
2287.5	0	3.8 (0)	2.281	35.05	23.05	I_{5V} = 73
	45	-30.3 (34.1)	2.253	34.57	22.57	
	90	-90.9 (94.7)	1.160	35.91	23.91	I_{12V} = 43
	135	-127.9 (131.7)	1.583	35.17	23.17	
	180	177.5 (186.3)	1.794	35.24	23.24	I_{22V} = 680
	225	140.5 (223.3)	1.710	35.08	23.08	
	270	86.7 (277.1)	1.306	35.89	23.89	
	315	52.2 (311.6)	1.749	35.16	23.16	

* Current measured at 0° phase setting only.

SIZE	CODE IDENT NO.	DRAWING NO.
A	96214	SKDD102
SCALE	REV	SHEET 11

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Table I. Transmitter Data Continued
(Room Temperature)

Input Power Level = +13 dBm

Frequency MHz	Commanded Phase Setting Degrees	Measured Phase Setting Degrees	Input VSWR	Power Output dBm	Gain dB	Power Supply* Currents mA
2217.5	0	11.7 (0)	1.304	36.15	23.15	I_{5V} = 93
	45	-26.6 (38.3)	1.039	35.98	22.98	
	90	-78.6 (90.3)	1.532	35.89	22.89	I_{12V} = 41
	135	-109.8 (121.5)	1.495	35.81	22.81	
	180	-178.3 (190)	1.238	35.58	22.58	I_{22V} = 915
	225	118.7 (308)	1.076	35.57	22.57	
	270	97.6 (294.1)	1.291	35.81	22.81	
	315	65.3 (316.4)	1.180	35.77	22.77	
2252.5	0	-176.7 (0)	1.479	36.71	23.71	I_{5V} = 93
	45	137.9 (45.4)	1.745	36.62	23.62	
	90	96.7 (86.6)	1.336	36.71	23.71	I_{12V} = 43
	135	51.4 (131.9)	1.165	36.58	23.58	
	180	-.2 (183.5)	1.190	36.47	23.47	I_{22V} = 900
	225	-44.9 (228.2)	1.061	36.63	23.63	
	270	-84.9 (269.2)	1.062	36.49	23.49	
	315	-129.2 (312.5)	1.408	36.32	23.32	
2287.5	0	-2.6 (0)	2.027	36.02	23.02	I_{5V} = 93
	45	-39.1 (36.5)	2.077	35.97	22.97	
	90	-91.4 (82.8)	1.036	36.22	23.22	I_{12V} = 43
	135	-133.4 (130.8)	1.420	35.96	22.96	
	180	176.3 (181.1)	1.496	35.75	22.75	I_{22V} = 745
	225	141.4 (216)	1.420	35.59	22.59	
	270	85.0 (272.4)	1.158	36.24	23.24	
	315	46.1 (311.3)	1.554	35.96	22.96	

* Current measured at 0° phase setting only.

SIZE	CODE IDENT NO	DRAWING NO
A	96214	SKDD102
SCALE	REV	SHEET 12

Table I. Transmitter Data Continued
(Room Temperature)

Input Power Level = +14 dBm

Frequency MHz	Commanded Phase Setting Degrees	Measured Phase Setting Degrees	Input VSWR	Power Output dBm	Gain dB	Power Supply* Currents mA
2217.5	0	14.6 (0)	1.487	35.92	21.92	I_{5V} = 73
	45	-22.9 (47.5)	1.145	35.83	21.93	
	90	-77.5 (92.1)	1.537	35.79	21.79	I_{12V} = 41
	135	-107.5 (122.1)	1.604	35.69	21.69	
	180	-175.7 (190.3)	1.390	35.40	21.40	I_{22V} = 915
	225	149.6 (225)	1.218	35.42	21.42	
	270	99.2 (275.4)	1.394	35.59	21.59	
	315	66.9 (307.7)	1.321	35.61	21.61	
2252.5	0	-174.7 (0)	1.428	36.64	22.64	I_{5V} = 73
	45	139.6 (45.7)	1.460	36.67	22.67	
	90	96.4 (88.9)	1.204	36.69	22.69	I_{12V} = 43
	135	53.3 (132)	1.308	36.56	22.56	
	180	+0.6 (184.7)	1.024	36.56	22.56	I_{22V} = 920
	225	-43.4 (228.7)	1.133	36.58	22.58	
	270	-87.8 (273.1)	1.194	36.50	22.50	
	315	-128.6 (313.9)	1.417	36.34	22.34	
2287.5	0	-5.9 (0)	1.675	36.5	22.5	I_{5V} = 73
	45	-39.4 (33.5)	1.689	36.19	22.19	
	90	-92.0 (86.1)	1.153	36.36	22.36	I_{12V} = 43
	135	-134.1 (128.2)	1.310	36.24	22.24	
	180	173.7 (180.4)	1.302	36.19	22.19	I_{22V} = 820
	225	137.7 (216.4)	1.260	35.97	21.97	
	270	89.6 (264.5)	1.251	36.23	22.23	
	315	45.6 (308.5)	1.329	36.17	22.17	

* Current measured at 0° phase setting only.

SIZE	CODE IDENT NO	DRAWING NO
A	96214	SKDD102
SCALE	REV	SHEET 13

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Table II. Recorded Receiver Phase and Gain Data
(Room Temperature Only)

Input Power Level = -40 dBm

Frequency MHz	Commanded Phase Setting Degrees	Measured Phase Setting Degrees	Input VSWR	Gain dB	Time Delay nsec	Power Supply* Currents mA
2030.9	0	-47, (0)	2.988	35.40	15.59	I_{5V} = 73
	45	-89.8 (42.8)	2.911	35.21	15.68	
	90	-137, (90)	2.723	34.42	14.80	I_{12V} = 42.5
	135	-173.6 (126.6)	2.322	33.87	14.506	
	180	125.3 (187.7)	2.487	34.04	14.51	
	225	[illegible] (226)	2.362	[illegible]	15.298	
	270	46.3 (272.7)	2.494	34.54	15.429	
	315	.3 (312.9)	2.[illegible]	[illegible]	15.117	
2041.9	0	-108.7 (0)	3.059	34.74	13.99	I_{5V} = 73
	45	-151.9 (43.2)	2.999	34.52	13.34	
	90	164.4 ([illegible])	3.026	34.05	13.122	I_{12V} = 43
	135	129. (122.3)	2.797	33.85	14.304	
	180	67.4 (183.9)	2.817	34.20	13.982	
	225	26.4 (224.9)	2.635	34.52	13.462	
	270	-20.7 (272)	2.77	34.56	13.69	
	315	-[illegible]5 (310.8)	2.[illegible]	34.65	14.671	
2052.9	0	-163.8 (0)	3.178	34.16	12.197	I_{5V} = 73
	45	155.3 (44.9)	3.209	34.04	12.55	
	90	112.4 (83.8)	3.495	33.47	13.187	I_{12V} = 42
	135	172.4 (123.8)	3.45	33.5	13.809	
	180	12.0 (184.2)	3.231	33.99	12.298	
	225	-28.9 (225.1)	3.147	34.57	13.27	
	270	-75. (271.2)	3.223	34.22	13.293	
	315	-117.6 (313.8)	3.127	34.29	13.269	

* Current measured at 0° phase setting only.

SIZE	CODE IDENT NO.	DRAWING NO.
A	96214	SKDD102
SCALE	REV	SHEET 14

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Table II. Receiver Data Continued
(Room Temperature)

Input Power Level = -40 dBm

Frequency MHz	Commanded Phase Setting Degrees	Measured Phase Setting Degrees	Input VSWR	Gain dB	Time Delay nsec	Power Supply* Currents mA
2074.15	0	99.5 (0)	2.087	33.42	13.24	I_{5V} = 93
	45	53.9 (45.6)	2.275	33.72	13.30	
	90	8.7 (90.8)	2.619	33.61	13.53	I_{12V} = 43
	135	-33.7 (133.2)	2.827	33.48	13.485	
	180	-86.5 (186)	2.517	33.84	13.282	
	225	-132.3 (231.8)	2.459	33.96	13.026	
	270	-177.1 (276.6)	2.369	33.63	12.696	
	315	141.3 (318.2)	2.31	33.43	13.277	
2095.4	0	-4.7 (0)	1.947	34.22	14.34	I_{5V} = 93
	45	-52.9 (42.2)	1.894	33.94	14.16	
	90	-99.9 (95.2)	1.912	33.54	13.55	I_{12V} = 43
	135	-140.2 (135.5)	2.158	33.1	12.87	
	180	170.5 (184.8)	2.156	33.89	13.692	
	225	125.1 (230.2)	2.162	33.41	13.511	
	270	79.4 (275.9)	2.264	33.29	13.019	
	315	39.9 (317.6)	2.125	33.28	12.867	
2106.4	0	-61.5 (0)	1.838	34.79	16.45	I_{5V} = 93
	45	-109. (47.5)	1.602	34.37	15.52	
	90	-153.6 (92.1)	1.488	33.73	15.44	I_{12V} = 43
	135	168.8 (129.7)	1.734	33.23	15.84	
	180	116.4 (181.1)	1.821	34.03	15.628	
	225	71.6 (226.9)	1.895	33.79	14.79	
	270	27.8 (270.7)	1.812	33.87	15.438	
	315	-13.3 (311.8)	1.889	33.67	15.832	

* Current measured at 0° phase setting only.

SIZE	CODE IDENT NO.	DRAWING NO.
A	96214	SKDD102
SCALE	REV	SHEET 15

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Table II. Receiver Data Continued
(Room Temperature)

Input Power Level = -40 dBm

Frequency MHz	Commanded Phase Setting Degrees	Measured Phase Setting Degrees	Input VSWR	Gain dB	Time Delay nsec	Power Supply* Current (mA)
2117.4	0	-126.6 (0)	2.363	34.88	16.45	I_{5V} = 73
	45	-170.5 (43.9)	1.897	34.04	15.52	
	90	145.3 (88.1)	1.605	33.43	15.44	I_{12V} = 43
	135	106.1 (127.3)	1.488	33.51	15.84	
	180	54.5 (178.9)	1.782	34.3	15.628	
	225	13. (220.4)	1.893	34.17	14.79	
	270	-33.3 (266.7)	1.813	34.15	15.497	
	315	-7[illegible] (309.4)	1.881	34.32	15.832	

* Current measured at 0° phase setting only.

SIZE	CODE IDENT NO.	DRAWING NO.
A	96214	SKDD102
SCALE	REV	SHEET 16

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Table III. Additional Receiver Test Data (Noise Figure, Compression, and Duplex Operation, Room Temperature Only)

Frequency MHz	Noise Figure dB	Noise Temperature °K	Output 1 dB Compression Point dBm	Transmit Signal Level From Receiver Under Duplex Operation (dBm)
2030.9	10.9 (4.9)	606	+9.45	--------
2041.9	10.95 (4.95)	617	+9.75	--------
2052.9	11.1 (5.06)	640	+10.0	--------
2074.15	10.85 (4.81)	588	+10.3	--------
2095.4	10.15 (4.05)	447	+10.45	--------
2106.4	10.2 (4.1)	456	+10.45	--------
2117.4	10.35 (4.16)	466	+9.5	--------
				1.6:1
2217.5	-----	-----	+10.3 dBm	+8.0 dBm
2252.5	-----	-----	+8.5	-2.0
2287.5	-----	-----	-8.1	-8.2

SIZE	CODE IDENT NO.	DRAWING NO.
A	96214	SKDD102
SCALE	REV	SHEET 17

APPENDIX C

APPENDIX C

TRANSMIT/RECEIVE MICROELECTRONICS MODULE

DESIGN SPECIFICATION

1.0 MODULE TECHNICAL REQUIREMENTS

1.1 Transmitter

1.1.1 Bandpass Characteristics

1.1.1.1 Center Frequency

The nominal center frequency shall be f_T = 2252 MHz.

1.1.1.2 Bandpass

$\pm$ 55 MHz centered at f_T (1 dB - BW)

1.1.1.3 Bandshape

The bandshape shall be such that the output signal level described in Paragraph 1.1.2.2.2 is achieved at each of the frequencies described in Paragraph 1.1.2.1.1, and that the response $\pm$ 2304 KHz from either of the frequencies described in Paragraph 1.1.2.1.1 varies less than 0.5 dB.

1.1.1.4 Response 100 MHz from Center of Bandpass

Attenuation at $\pm$ 100 MHz from f_T is more than 10 dB with respect to response at f_T.

1.1.1.5 Response 150 MHz from Center of Bandpass

Attenuation at $\pm$ 150 MHz from f_T is more than 20 dB with respect to response at f_T.

1.1.2 Signal Characteristics

1.1.2.1 Input Signal

1.1.2.1.1 Type

The input signal shall be a single angle modulated carrier operating at either one of two carrier frequencies, 2217.5 or 2287.5 MHz.

1.1.2.1.2 Modulation Width

The extent of the input signal spectrum shall be 2304 KHz from the carrier frequency to the second null of the spectrum.

1.1.2.1.3 Power Level

The input transmit signal at the input connector of each transceiver module shall be 13 dBm $\pm$ 1 dB.

1.1.2.2 Output Signal

1.1.2.2.1 Characteristics

The output signal shall be a replica of the single carrier input signal within the bandwidth of Paragraph 1.1.1.2.

1.1.2.2.2 Transceiver Module Power Output

The output power from each module at either frequency of Paragraph 1.1.2.1.1 will be no less than 35 dBm when terminated in a nominal 50 Ω load having a VSWR no greater than 1.5:1.

1.2 Receiver

The specifications for the receiver portion of the system are limited to the transceiver modules inasmuch as the system tests which validate the receiver performance are not included in this scope of work.

1.2.1 Bandpass Characteristics

The receiver has two frequency bands: one in S-band nominally centered at 2074 MHz (f_{RS}) and one in L-band nominally centered at 1804 MHz (f_{RL}). Only the center module will have an L-band frequency lead. The bandpass centered about the above center frequencies will be the following:

1.2.1.1 S-band Bandpass

87 MHz centered at f_{RS} (0.5 dB - BW).

1.2.1.2 L-band Bandpass

62 MHz centered at f_{RL} (0.5 dB - BW)

1.2.1.3 S-band Bandshape

The bandshape shall be such that the gain (described in Paragraph 1.2.2.2 and noise temperature described in Paragraph 1.2.2.4 shall be achieved at each of the S-band frequencies described in Paragraph 1.2.2.1) varies less than 0.5 dB.

1.2.1.4 L-band Bandshape

The bandshape shall be such that the loss described in Paragraph 1.2.2.3 and the noise temperature described in Paragraph 1.2.2.5 shall be achieved at each of the L-band frequencies described in Paragraph 1.2.2.1.1 and the response $\pm$ 2304 KHz from either of the L-band frequencies described in Paragraph 1.2.1.1 varies less than 0.5 dB. Only the center module has L-band capability.

1.2.1.5 Attenuation at $f_{RS} \pm 100$ MHz from f_{RS} is no less than 15 dB with respect to carrier with 20 dB as a design goal.

1.2.1.6 Attenuation at $f_{RS} \pm 140$ MHz from f_{RS} is no less than 40 dB with respect to the carrier with 45 dB as a design goal.

1.2.1.7 Attenuation at $f_{RS} \pm 250$ MHz from f_{RS} is no less than 60 dB with respect to the carrier.

1.2.2 Signal Characteristics

1.2.2.1 Input Signal

The input signal shall be a single angle modulated signal operating at a frequency of 2041.9, 2106.4, 1775.5 or 1831.8 MHz. The bandwidth of the L-band signal is at most $\pm$ 2.304 MHz from the carrier frequency to the second null. The S-band signal bandwidth when receiving from the ground system will be at most 4.6 MHz between second nulls. The S-band signal bandwidth when receiving from the Tracking and Data Relay Satellite shall be 22 MHz.

1.2.2.2 S-Band Receive Electronic Gain

The electronic gain to all signals in the S-band signal bandpass of Paragraph 1.2.1.1 shall be greater than 25 dB. This gain is measured from the antenna port of a single transceiver module to the S-band output port up to an output signal level of 0 dBm.

1.2.2.3 L-Band Electronic Loss

The L-band electronic loss shall be less than 4 dB between the antenna connector of the central module to the L-band output port.

1.2.2.4 Noise Temperature (S-band)

The S-band transceiver module noise temperature referenced to the module antenna connector shall be less than 700°K with a design goal of 600°K over any 10 MHz in the bandpass described in Paragraph 1.2.1.1 when terminated into a 50 ohm load at the S-band output connector.

1.2.2.5 Noise Temperature (L-band)

The L-band noise temperature of the S-band antenna sub-system referenced to the center module antenna connector shall be less than 440°K over any 10 MHz in the bandpass described in Paragraph 1.2.1.2 when terminated into a 50 ohm load.

1.3 Suitable Module Temperature Range

To meet all module power, gain, noise figure and phase requirements, the maximum module case temperature range is 0°C to +45°C.